8.1 Microwave Semiconductor Devices

The microwave frequency range, which extends from 1GHz(10^9 Hz) upto 100 GHz and further, is becoming more and more important in 'modern' communication systems. Also, nanosecond (10^{-9} sec) response is a major demand in 'modern' computer systems. The first active semiconductor device, especially intended for microwave use, appeared about 30 years ago. More advance such devices are gaining control of this field in the low power (upto a few watts) part of it. The high-power microwave field is *still dominated* by vacuum tubes. The requirements for high power and high frequency, *at present*, are contradictory in many aspects of the semiconductor-device design.

8.1.1 Schottky Barrier Diode

The first semiconductor device was a rectifier made by using a metal whisker contacting a piece of semiconductor material. Such an arrangement is called a *metal-semiconductor junction* (or contact).

When two substances are brought into contact, a redistribution of charge occurs; finally a new equilibrium condition is reached where the Fermi levels of the two substances are at equal heights (chapter 2). This rule holds not only for contacts between two metals but also for the contact between a metal and a semi-conductor. A *dipole layer* is formed at the contact owing to the redistribution of charge. In a metal-metal contact this dipole layer is always caused by *surface charges* on both sides of the contact; such a contact is an *ohmic contact*, since the electrons can move freely from one metal into the other. However, the contact may be either ohmic or *rectifying* in a metal-semiconductor contact. By rectifying contact we mean that current flows much more easily in one direction than in the opposite one.

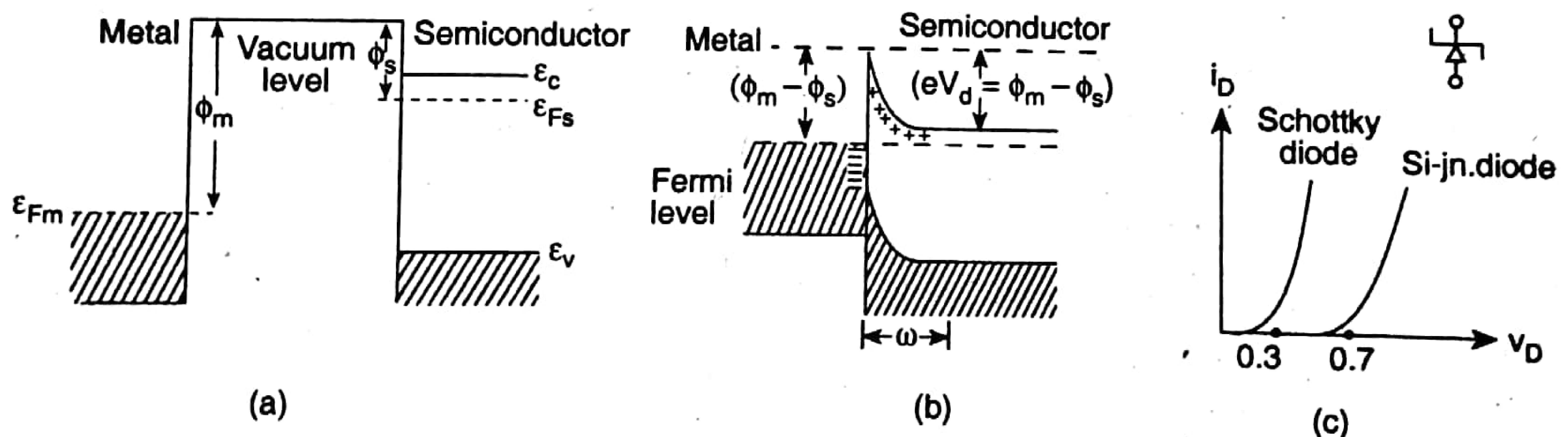

Fig. 8.1 Schottky barrier diode (a) Energy-level diagram with $\phi_m > \phi_s$ before contact, (b) Energy level diagram after contact for metal–*n*–type– semiconductor, (c) Symbol of a Schottky diode with characteristics

As an example, let us consider a contact between a metal with work function ϕ_m an n-type semiconductor with work function ϕ_s. Let also the donor concentration in the semiconductor be relatively large and let almost all donors be ionized at room temperature. We first consider the case $\phi_m > \phi_s$. Here, the semiconductor Fermi level ε_{FS} must initially be higher than that of the metal before the contact is made, as

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shown in Fig. 8.1(a). To align the two Fermi levels, the electrostatic potential of the semiconductor must be raised (i.e., the electron energies must be lowered) relative to that of the metal. Hence, an exchange of charge occurs—electrons from the surface layer of the semiconductor enter the metal, leaving behind ionized donors in that surface layer (for charge-neutrality condition). After the exchange of charge (electrons) is completed, the Fermi levels in both materials are at the same height. This means that the energy levels in the bulk semiconductor are lowered by an amount $(\phi_m - \phi_s)$. As a consequence a potential barrier is formed at the interface, and a dipole layer and a depletion region of width ω is created near the contact, as shown in Fig. 8.1(b). Expressed in volts, the height of the barrier follows from

$$\mathrm{e}V_d = \phi_m - \phi_s \tag{8.1.1}$$

The width of the *depletion* region depends upon the concentration of ionized donors and the magnitude of V_d.

Use of Boltzman statistics to calculate the number of those that have high enough energy, due to the application of an applied voltage V across the contact, to cross it gives the current that will flow as

$$I \doteq I_0 \left(\exp \frac{\mathrm{e}V}{\eta k T} - 1 \right) \tag{8.1.2}$$

where η is called the *ideality factor.* Owing to the thermal agitation some electrons of the metal will have sufficient energy to cross the potential barrier into the semiconductor and vice versa. In equilibrium this gives rise to equal and opposite currents I_0 crossing the barrier. Similar equation holds for a metal-p-type semiconductor contact. Such contacts are rectifying.

The class of contacts just described was originally investigated by W. Schottky of Germany, and the potential hill appearing in such cases is called the *Schottky barrier*, and the diodes utilizing it are called *Schottky-barrier diodes* or simply *Schottky diodes.* In the metal part of a Schottky diode, carrier storage (or the storage effect) is nonexistent in contrast to $p-n$ junctions, and hence Schottky diodes have a faster speed of response since there is no time lag associated with the *storage time* (defined as the time interval between the application of the reverse bias and cessation of the reverse current surge).

Though the current-voltage relation of a Schottky diode is similar to that of a *pn*-junction diode there are various differences between them :

(i) In a *pn*-junction diode the reverse leakage current is due to *minority* carriers diffusing to the depletion layer edges to be swept across to recombine; hence it is very temperature sensitive. For Schottky diodes it is the result of the *majority* carriers that overcome the barrier. That would give a much higher value of I_0 which is less sensitive to temperature.

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(ii) Under forward bias, the injection is from semiconductor only. Hence there is very little recombination in the depletion region and the ideality factor η is ~ 1 (1.03 is a practical value) while for pn-junctions $1.2 < \eta < 2$.

(iii) The cut-in voltage V_γ is ~ 0.3 V (comparable to Ge-diodes) but much less than Si-diode, (~ 0.7 V) (Fig. 8.1(c)).

(iv) The majority electrons injected over the Schottky barrier into the metal have much higher energy than the rest of the metal electrons which are in thermal equilibrium with metal lattice atoms. The injected electrons are therefore called *hot*, and the diodes are often called hot-electron diodes.

(v) The diffusion capacitance C_d is negligible in Schottky diodes. Only the depletion capacitance C_T (see section 2.3.5) appears in high-frequency model. Therefore, Schottky diode operate at a much higher frequency.

(vi) V-I characteristic of Schottky diode being steeper than pn-junction diode, its differential resistance $\frac{\partial V}{\partial I}$ is much less.

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Tunnel diode

A P-n junction device [2 sides are degenerate semi-conductor]
Si, SnSb, GaAs, PbTe.

Operates → in certain regions of its I-V characteristics.

→ Quantum Mechanical tunneling of electron through the Pn barrier of the junction.

To initiate this process :- A negligible reverse bias voltage is needed

Used : High speed switching and logic circuits.
Oscillation, amplification ckt.

other name . Esaki diode
↓
Received Nobel prize for this work on 1973.

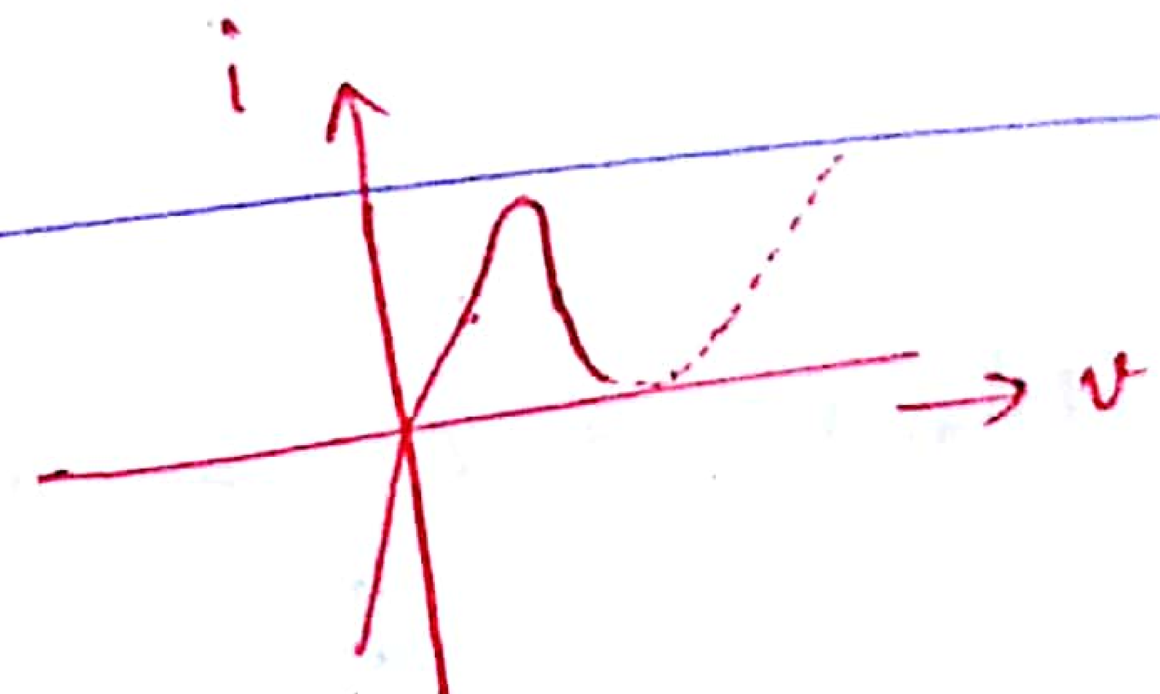
Important feature: Negative resistance over a portion of its I-V characteristics.

has not widespread application :- because of its relatively low current operation

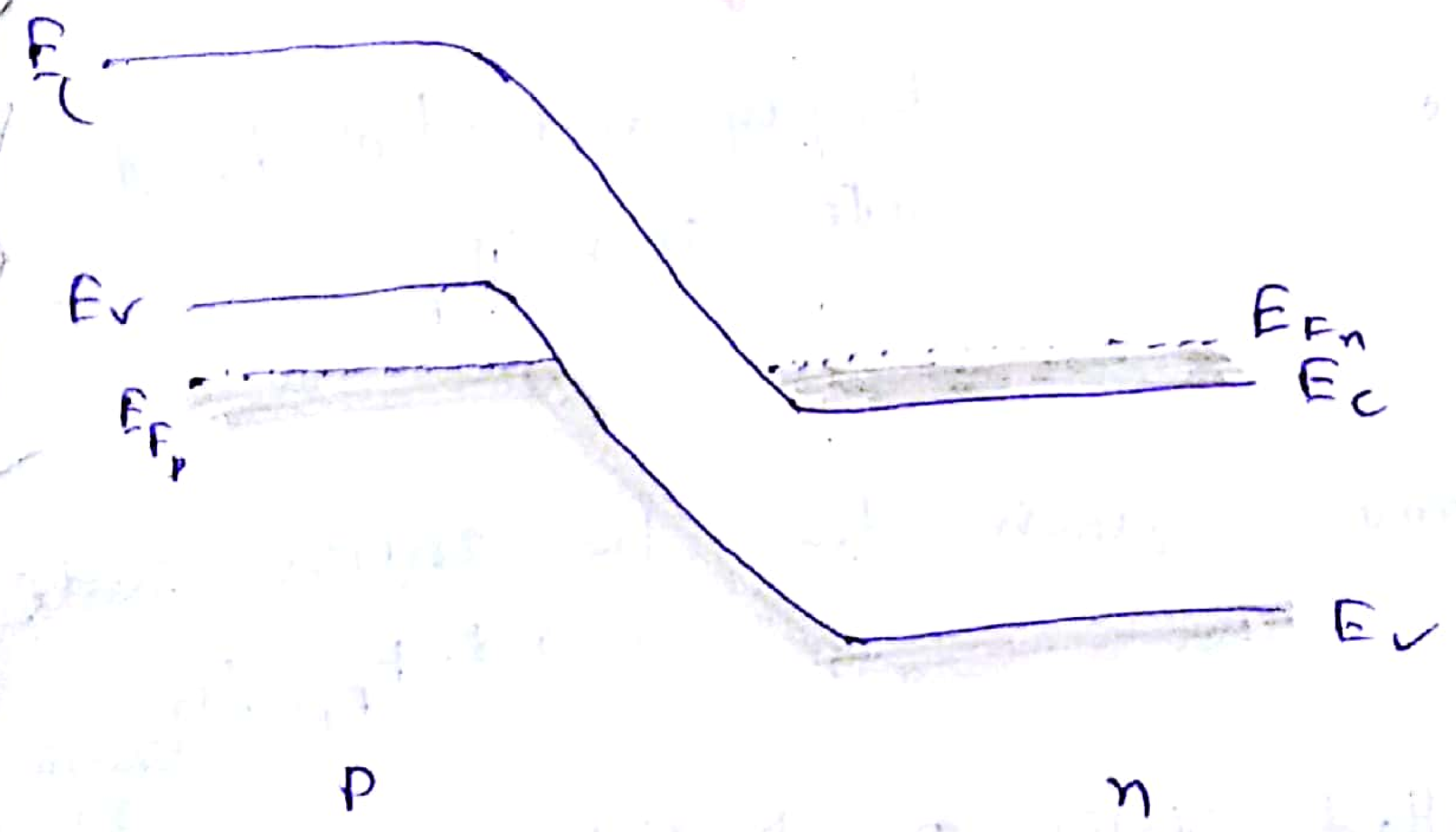
Tunnel process does not present the time delay of drift and diffusion . So, it is a good choice for high speed ckt

Normaly
Energy state → below E_F → mostly filled
" " → above E_F → " empty.

for degenerate n-type → Region betn E_C and E_F → filled with electrons
" p type → Region betn E_V & E_F → Filled with holes.



Tunnel diode operation



Equilibrium Condition

⇒ E_{Fp} → lies below VB edge on p side.

E_{Fn} → Above CB edge on n-side

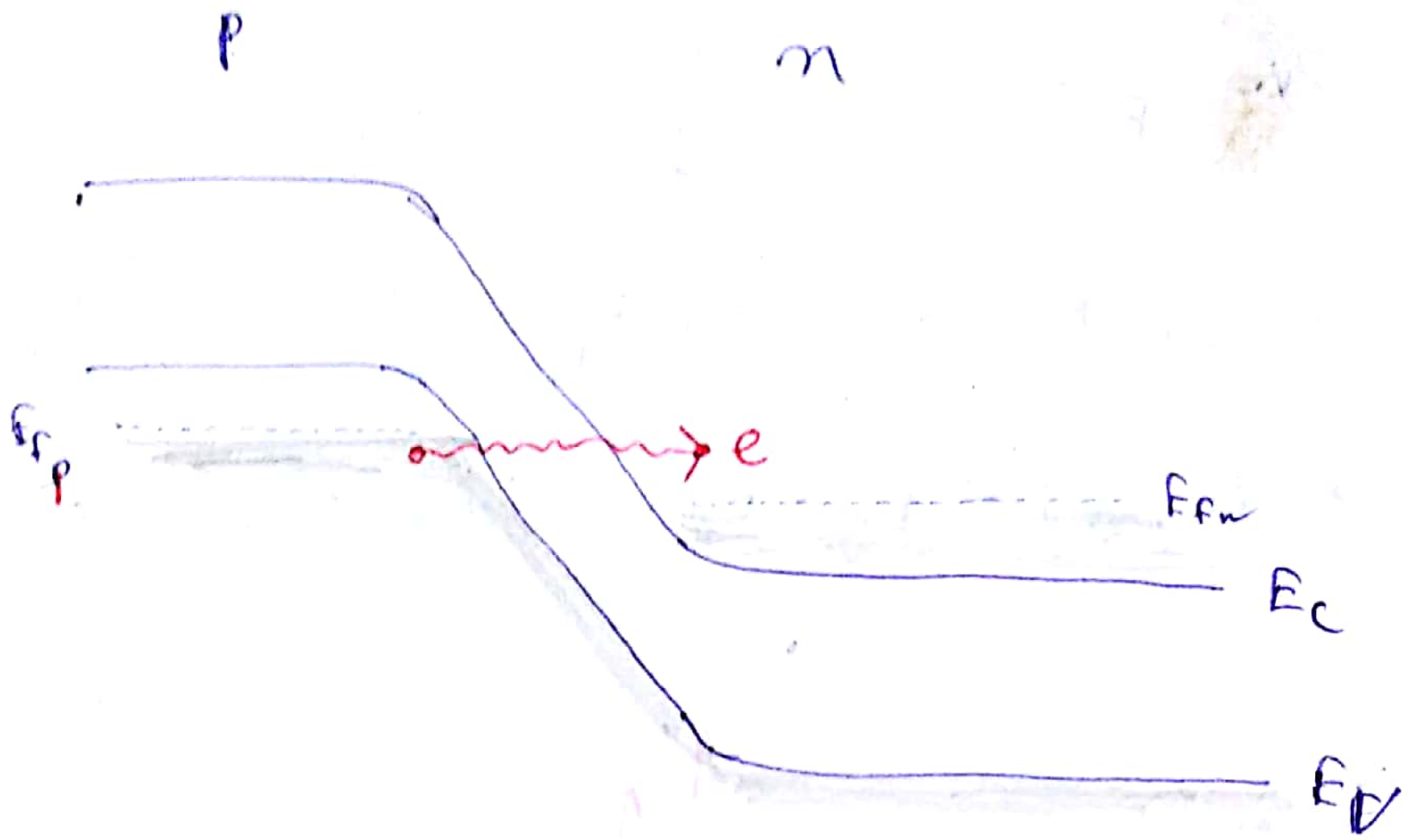
This means

VB & CB → must overlap each other.

Zero bias, No net tunneling

tunneling of e from n → p = tunneling of e from p → n.

In small reverse bias



Allows → e → tunneling from filled VB states below E_{F_p}

↓ To

Empty conduction band states above E_{F_n}

when RB increased

E_{F_n} → Continues move down the the energy scale w.r.t. E_{Fp} (By amount qV)

placing ⇒ more filled states on p-side

" ~~of~~ empty states on n-side.

Effect ⇒ increase tunneling of electron from p → n

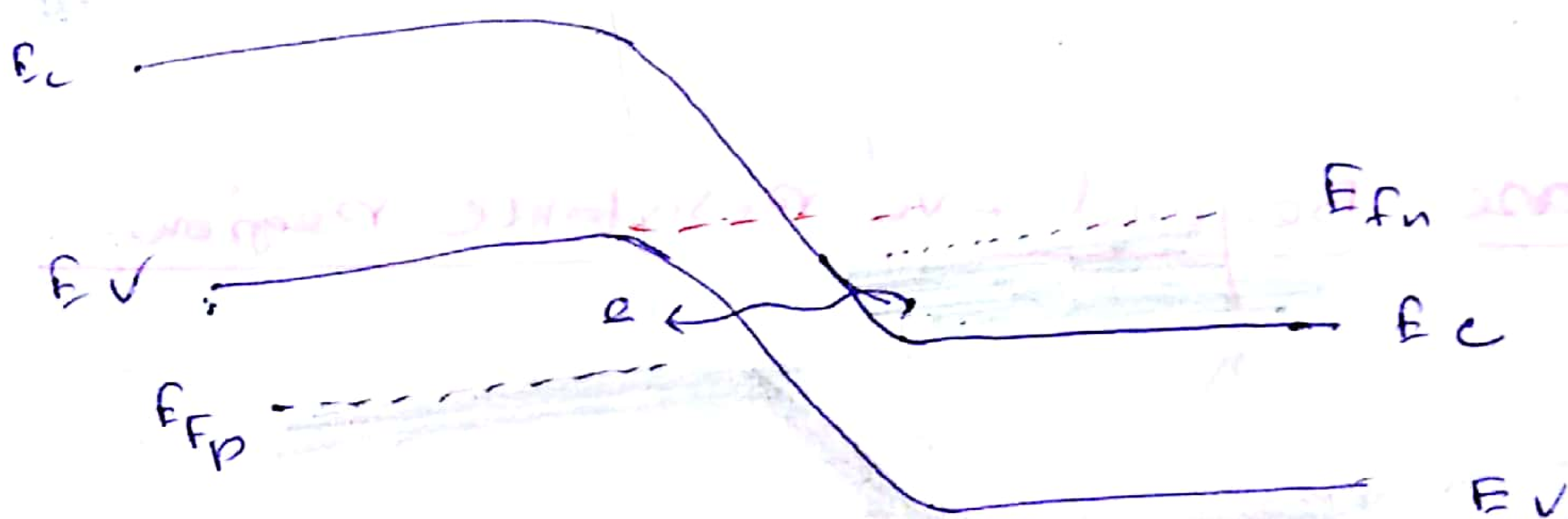
Resulting current increase (current from n to p)

In small Forward bias

- E_{Fn} → moves up by amount qV (w.r.t. E_{Fp})

Electron below → E_{Fn} → on n side
↓ tunnel to
p side.

current from ⟹ p to n side.



Forward tunneling current

increase → with increasing FB voltage
→
E_{Fn} → continue → to move up w.r.t. E_{Fp}.

A point reach: Bands begin to pass by each other.

When this occur

decrease → tunnel current.

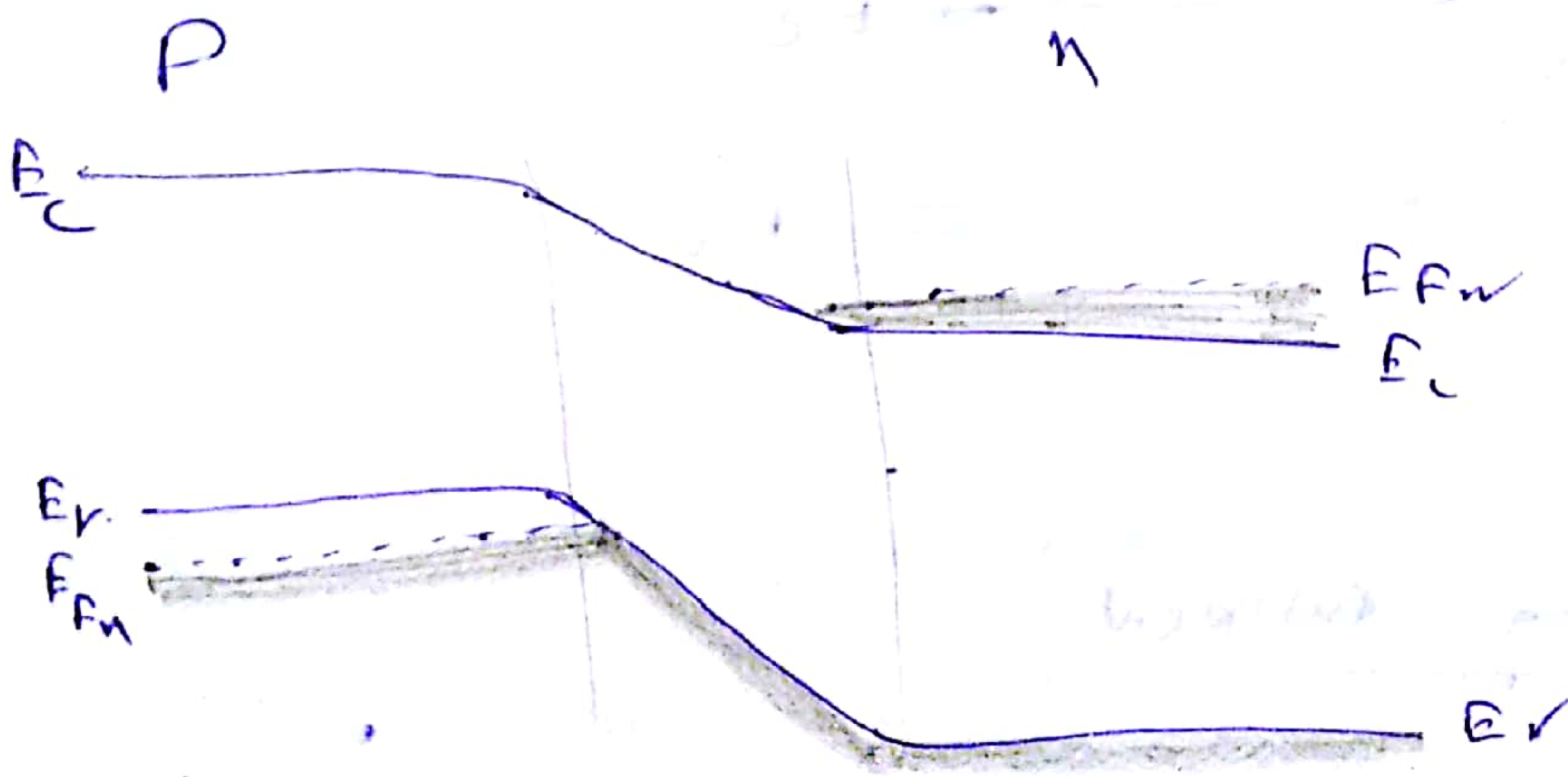
tunneling current decrease → with increasing FB voltage

⇒ Negative slope region in I-V charact.

i.e dynamic resistance : $\frac{dV}{dI}$ is −ve.

⇒ −ve resistance region,

FB increase Beyond −ve resistance region



Bands ⇒ completely passed each other

⇒ The diode ⇒ Resembles Conventional P-n diode.

Diffusion current Dominate over tunneling current.

In Forward tunneling →

tunneling current dominate over diffusion current.

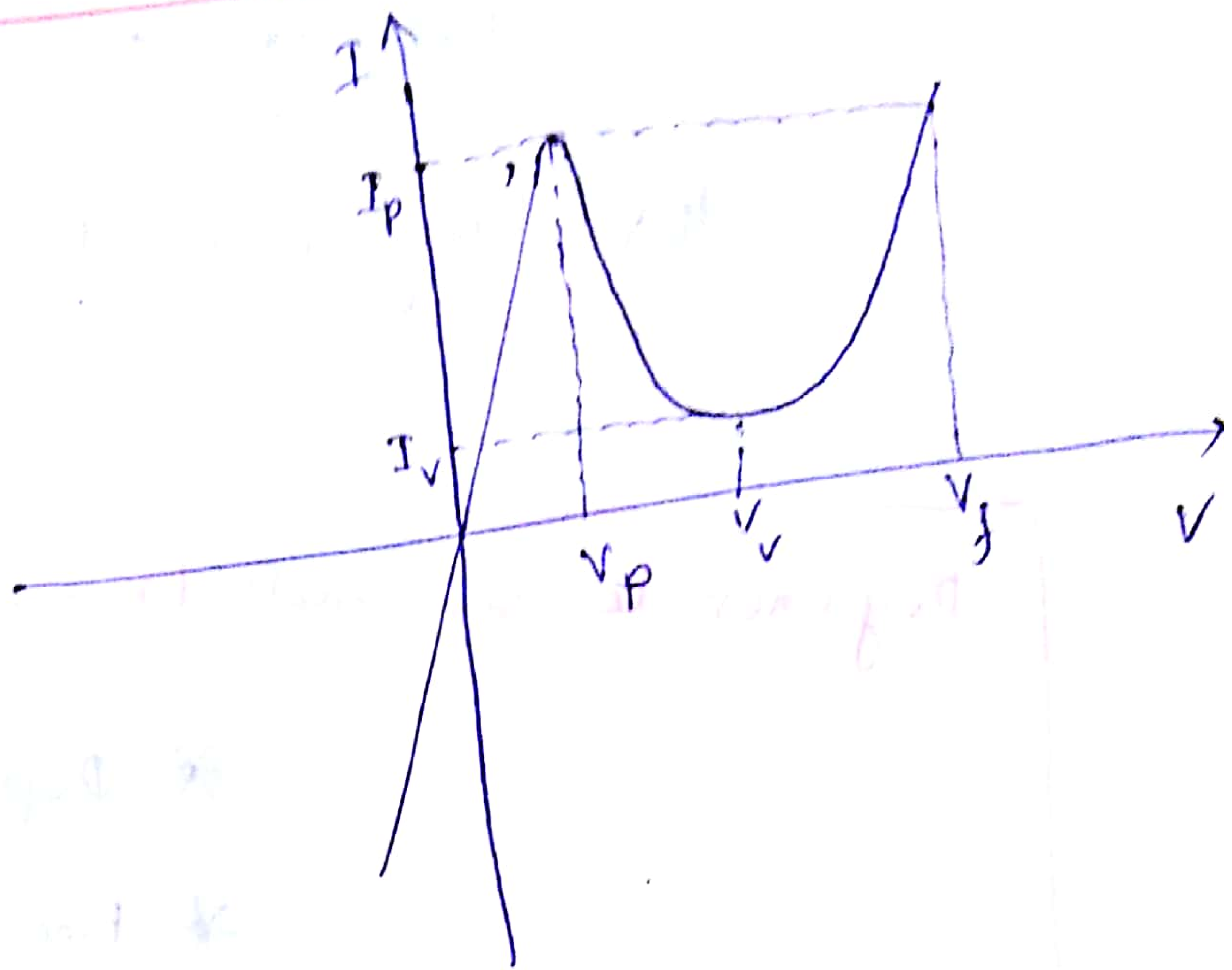
Degenerate semiconductor ⇒ doping high

* Depletion region → very sharp
* Elec. field at the junction → large

⇒ Condition for electron tunneling are met

Filled & empty states ⇒ separated by a narrow Pot^n. barrier of finite height

Tunnel diode characteristic



General shape: N

This characteristics: type N - negative resistance.

Also called: Voltage - controlled negative resistance

Peak voltage (V_p): After this voltage current decrease rapidly.

→ At this voltage forward tunneling become maximum.

Peak tunneling current (I_p)
Valley current (I_V)
→ I_p & I_V → determine the magnitude of -ve resistance slope for a diode of given material

Figure of merit for tunnel diode $\rightarrow = \frac{I_P}{I_V}$ → determine the magnitude of the -ve resistance slope for the diode.

Voltage spread between two +ve resistance regions $\rightarrow = \frac{V_P}{V_f}$

Peak voltage V_P
Valley voltage V_V

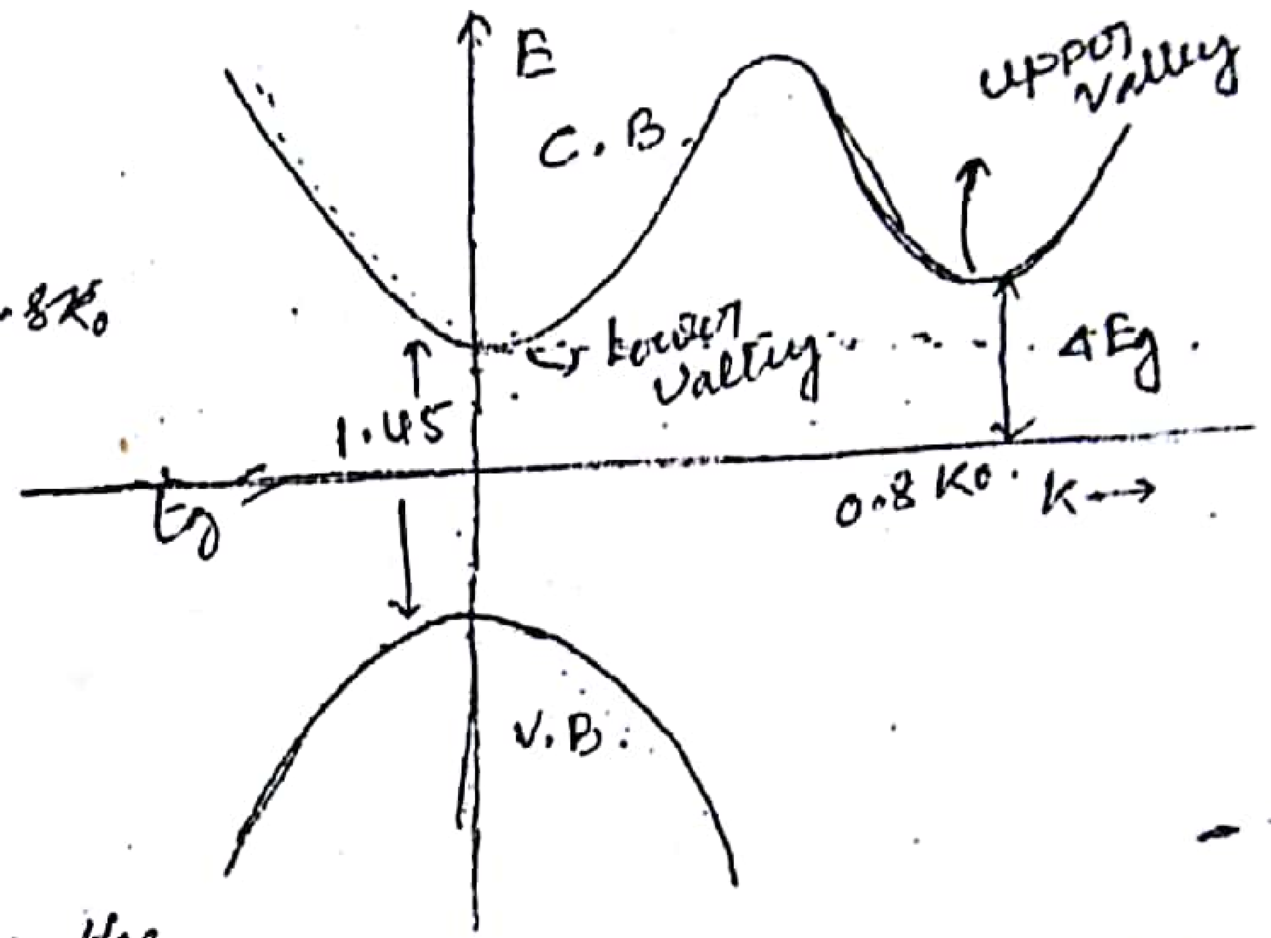
$\Delta V = V_P - V_V$ ⇒ called voltage swing

At 300°K (27°C) ⇒	For GaAs tunnel diode	For Ge tunnel diode
V_P =	200mV	100mV
V_V =	600mV	300mV

Gunn diode

Electron - Gas Heating :

Ohm law is obeyed by most homogenious Semiconductor over a wide range of current density J and electric - field intensity E so long the carriers do not go far out of thermal equilibrium : The situation become quite interesting when they aquire scattering limited velocity with rising electric field. For certain semiconductor like GaAs a portion of the V_d vs E characteristic then displace negative conductance property which is normally unstable.



The diagram shows two minima. one at $K = 0$ and the 2nd one is at $K = 0.8K_0$ where K_0 is the wave vector corresponding to Brillouin zone boundaries. The 2nd minima lies at 0.36 eV about the 1st ($\Delta E_g = 0.36$ eV).

At normal electric field interestingly there could be practically no electron in the upper valley. In the lower valley $m_e^* = 0.07\,m$ for electron e mobility $= 0.5\,V/m^2\text{-}s$. On exposure of a crystal to an electric field electron gather a drift velocity $v_d = \mu_L E$ and grow in proportion to electric field E.

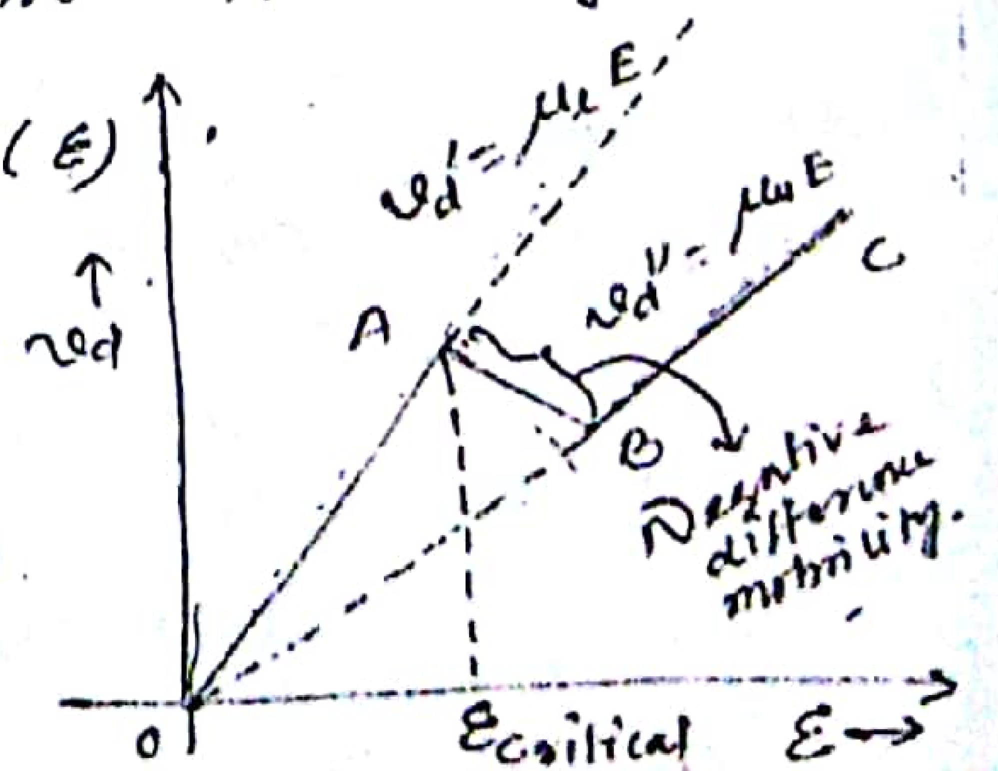
The electron get enough energy to be transferred to the upper valley at a field of the order of 10^5 V/m.

In the upper valley $m_u^* = 1.2\,m$

$\mu_u = 0.01\,V/m^2\text{-}s$

Now the drift velocity of electron drop sharply as they make this transition because their mobility decreases. The effect shows the appearance of the portion AB of negative differential mobility. After the main body of electron has move to the upper valley.

A further rise in the electric field (E) will cause proportional rise in the drift velocity $v_d'' = \mu_u E$.



This is shown in the portion BC. The appearance of the portion of negative differential mobility in GaAs is made use of design microwave oscillators. The state in the upper valley is unstable. The electron interact with phenomenon and go over the lower valley increasing the current. Periodic oscillation starts as we apply critical field GaAs.

The frequency of current oscillation is $1.6 \times 10^{+9} s^{-1}$ and amplitude may exceed 1 amp. High frequency current oscillation in semiconductor accompanying the application of constant voltage is known as Gunn effect. This effect is observed in GaAs, GaP and some other solid. Gunn effect observed in a material which is not a diode current oscillation when a voltage pulse of 16 volts and 10^{-8} s duration has been applied to n-type GaAs of 0.025 mm length.

If (n_l, v_l) and (n_u, v_u) are the electron densities and drift velocity respectively in the lower and upper valley the average drift velocity of the electron may be expressed as—

$$v_d = \frac{n_l v_l + n_u v_u}{(n_l + n_u)}$$

where, $v_l = \mu_l \varepsilon$

$v_u = \mu_u \varepsilon$

$$v_d = \frac{n_l \mu_l \varepsilon + \mu_u n_u \varepsilon}{(n_l + n_u)}$$

$$= \frac{\mu_l + \left(\frac{n_u}{n_l}\right)\mu_u}{\left(1 + \frac{n_u}{n_l}\right)} \cdot \varepsilon \longrightarrow (1)$$

Again,

$$n_u = N_{cu}\, e^{(E_F - E_{cu})/KT}$$

$$n_l = N_{cl}\, e^{(E_F - E_{cl})/KT}$$

$$\therefore \left(\frac{n_u}{n_l}\right) = \left(\frac{N_{cu}}{N_{cl}}\right) e^{(E_F - E_{cu} - E_F + E_{cl})/KT}$$

$$= \left(\frac{N_{cu}}{N_{cl}}\right) e^{(E_{cl} - E_{cu})/KT}$$

$$= \frac{N_{cu}}{N_{cl}} e^{-\Delta E_g/KT} \quad \text{where } \Delta E_g = (E_{cu} - E_{cl}) \longrightarrow (2)$$

Putting eq's (2) from eq's (1), we get.

$$v_d = \frac{\mu_l + \mu_u \left(\frac{N_{cu}}{N_{cl}}\right) e^{-\Delta E_g/KT}}{\left(1 + \frac{N_{cu}}{N_{cl}} e^{-\Delta E_g/KT}\right)} \cdot \varepsilon$$

When the electron energy becomes is very high it is no longer in thermal equilibrium in lattice. At this stage the electron temp. T_e must be distinguish from the lattice temp. T_0

$$v_d = \frac{\mu_l + \mu_u \left(\frac{N_{cu}}{N_{cl}}\right) e^{-\Delta E_g/KT_e}}{1 + \left(\frac{N_{cu}}{N_{cl}}\right) e^{-\Delta E_g/KT_e}} \varepsilon \longrightarrow (3)$$

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The excess thermal energy of Conduction electron over that of lattice is given by — $K(T_e - T_0)$ is transferred back to the latter as if there are an effective mean free path l of collision betn electron and photon. The rate of rise of electron temp. may be expressed as—

$$C\left(\frac{dT_e}{dt}\right) = qEv_d - \frac{K(T_e - T_0)}{(l/v_d)}$$ ⇒ Energy given to the lattice.

↓ Energy gain by electron through high electric-field.

In equilibrium, $\frac{dT_e}{dt} = 0$

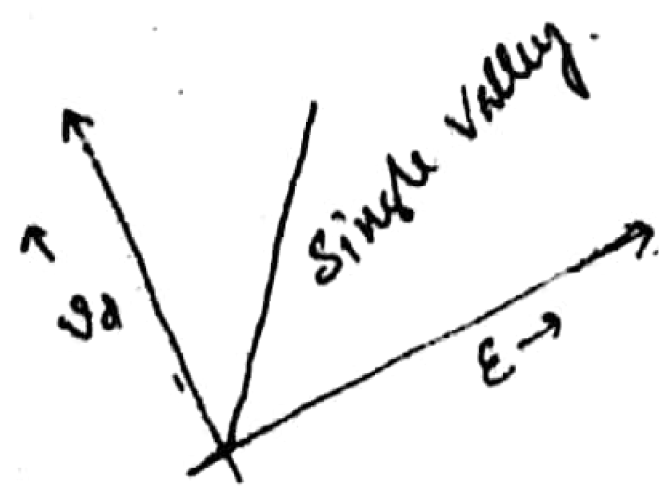
$$\therefore \boxed{T_e = T_0 + \left(\frac{ql}{K}\right)E} \longrightarrow (4)$$

Relation between electron temp. and lattice temp. strong electric-field.

For small electric-field intensity $T_e \simeq T_0$ and we have $\Delta E_g >> KT_e$ so in that case from eq's (5) we get,

$$\boxed{v_d = \mu_L E}$$

↳ drift velocity will be controlled by the mobility of electron in the lower valley.



On the other hand for larger electric-field, $T_e >> T_0$ we have

$\Delta E_g << KT_e$

From eq's (5).

$$\boxed{v_d = \mu_u E}$$

↳ Drift velocity will be controlled by mobility of the electron in the upper valley.

We ~~make~~ may now summarised the basic requirement to obtain the negative differential mobility region in the v_d vs E of a two valley conduction band of a semi-~~conductor~~ conductor.

(i) The higher energy upper valley must have an applicable larger effective mass than in the main conduction band. The negative mobility region is not marked until $\mu_L > 50\,\mu_u$.

(ii) The energy difference betn the main conduction band and the upper valley must be larger than the thermal energy of lattice i.e. $\Delta E_g > KT_0$.

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5.7.1 Schottky Barriers

In Section 2.2.1 we discussed the work function $q\Phi_m$ of a metal in a vacuum. An energy of $q\Phi_m$ is required to remove an electron at the Fermi level to the vacuum outside the metal. Typical values of Φ_m for very clean surfaces are 4.3V for Al and 4.8V for Au. When negative charges are brought near the metal surface, positive (image) charges are induced in the metal. When this image force is combined with an applied electric field, the effective work function is somewhat reduced. Such barrier lowering is called the *Schottky effect,* and this terminology is carried over to the discussion of potential barriers arising in metal–semiconductor contacts. Although the Schottky effect is only a part of the explanation of metal–semiconductor effects, rectifying contacts are generally referred to as *Schottky barrier diodes*. In this section we shall see how such barriers arise in metal–semiconductor contacts. First we consider barriers in ideal metal–semiconductor junctions, and then in Section 5.7.4 we will include effects which alter the barrier height.

When a metal with work function $q\Phi_m$ is brought in contact with a semiconductor having a work function $q\Phi_s$, charge transfer occurs until the Fermi levels align at equilibrium (Fig. 5-31). For example, when $\Phi_m > \Phi_s$, the semiconductor Fermi level is initially higher than that of the metal before contact is made. To align the two Fermi levels, the electrostatic potential of the semiconductor must be raised (i.e., the electron energies must be lowered) relative to that of the metal. In the n-type semiconductor of Fig. 5-31 a depletion region W is formed near the junction. The positive charge due to uncompensated donor ions within W matches the negative charge on the metal. The electric field and the bending of the bands within W are similar to effects already discussed for p-n junctions. For example, the depletion width W in the semiconductor can be calculated from Eq. (5-21) by using the p^+-n approximation

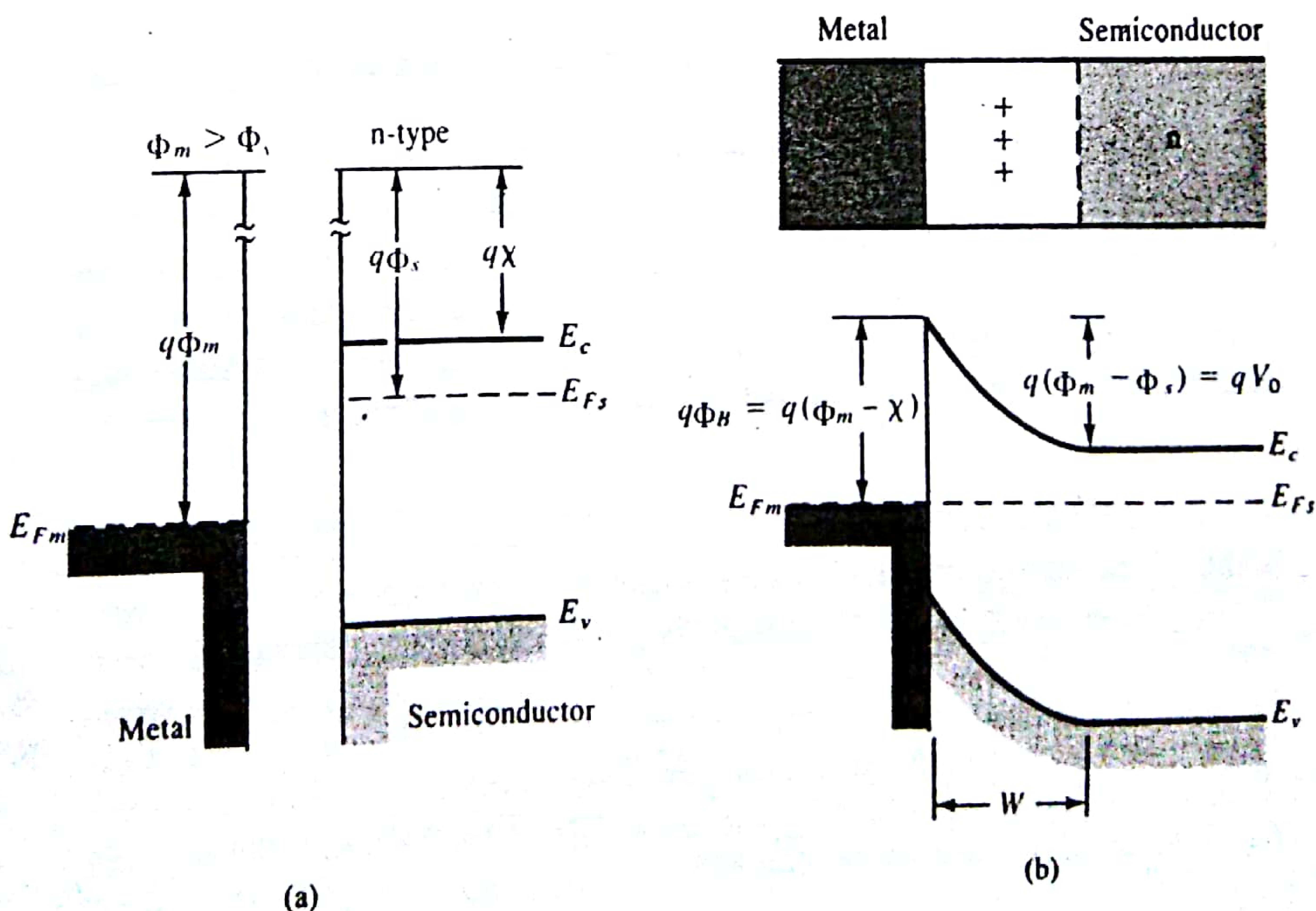

Figure 5-31 A Schottky barrier formed by contacting an n-type semiconductor with a metal having a larger work function: (a) band diagrams for the metal and the semiconductor before joining; (b) equilibrium band diagram for the junction.

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(i.e., by assuming the negative charge in the dipole is a thin sheet of charge to the left of the junction). Similarly, the junction capacitance is $A\epsilon_s/W$, as in the p^+-n junction.†

The equilibrium contact potential V_0, which prevents further net electron diffusion from the semiconductor conduction band into the metal, is the difference in work function potentials $\Phi_m - \Phi_s$. The potential barrier height Φ_B for electron injection from the metal into the semiconductor conduction band is $\Phi_m - \chi$, where $q\chi$ (called the *electron affinity*) is measured from the vacuum level to the semiconductor conduction band edge. The equilibrium potential difference V_0 can be decreased or increased by the application of either forward- or reverse-bias voltage, as in the p-n junction.

Figure 5-32 illustrates a Schottky barrier on a p-type semiconductor, with $\Phi_m < \Phi_s$. In this case aligning the Fermi levels at equilibrium requires a positive charge on the metal side and a negative charge on the semiconductor side of the junction. The negative charge is accommodated by a depletion region W in which ionized acceptors (N_a^-) are left uncompensated by holes. The potential barrier V_0 retarding hole diffusion from the semiconductor to the metal is $\Phi_s - \Phi_m$, and as before this barrier can be raised or lowered by the application of voltage across the junction. In visualizing the barrier for holes, we recall from Fig. 5-7 that the electrostatic potential barrier for positive charge is opposite to the barrier on the electron energy diagram.

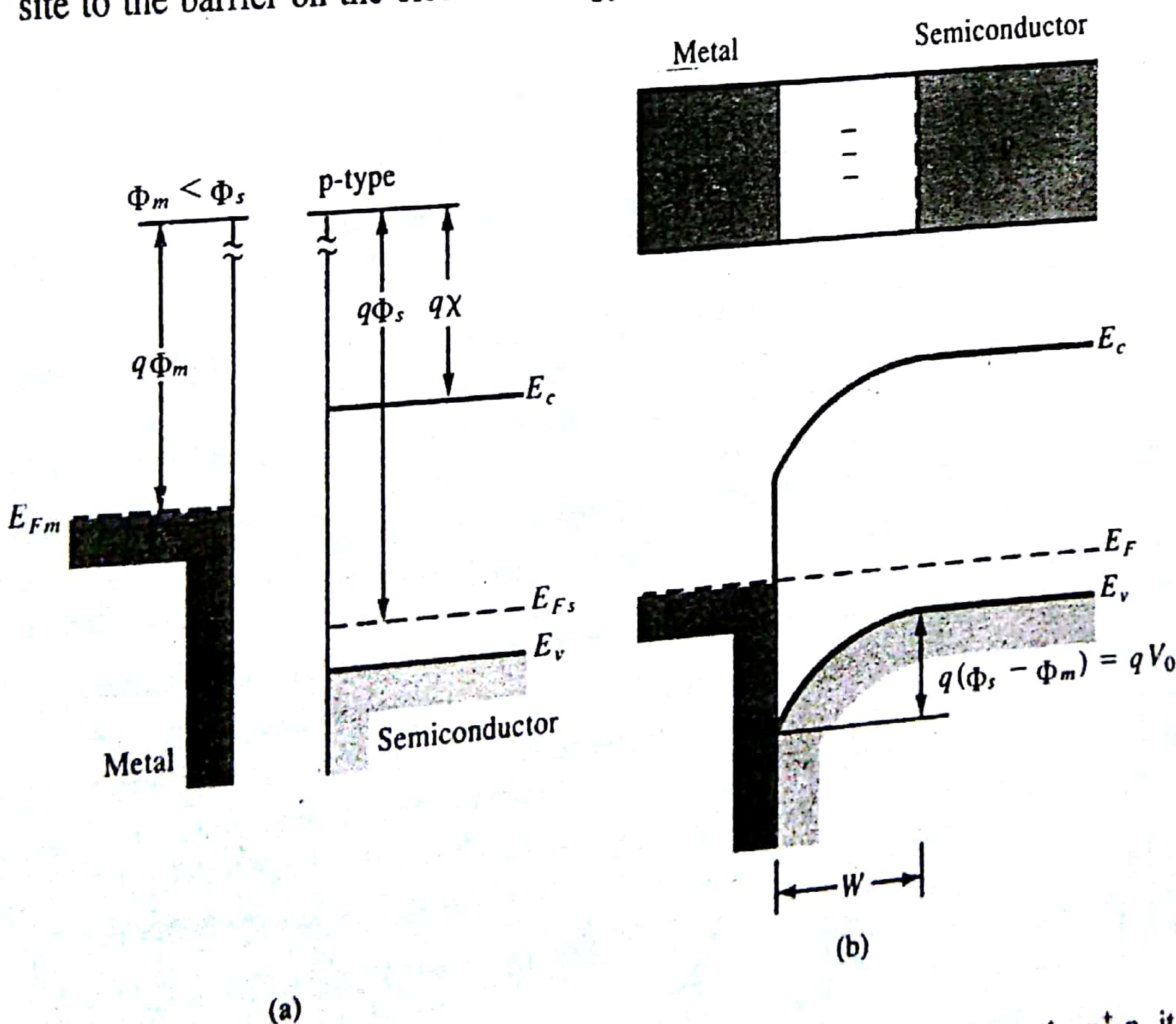

Figure 5-32 Schottky barrier between a p-type semiconductor and a metal having a smaller work function: (a) band diagrams before joining; (b) band diagram for the junction at equilibrium.

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†While the properties of the Schottky barrier depletion region are similar to the p^+-n, it is clear that the analogy does not include forward-bias hole injection, which is dominant for the p^+-n but not for the contact of Fig. 5-31.

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The two other cases of ideal metal-semiconductor contacts ($\Phi_m < \Phi_s$ for n-type semiconductors, and $\Phi_m > \Phi_s$ for p-type) result in nonrectifying contacts. We will save treatment of these cases for Section 5.7.3, where ohmic contacts are discussed.

5.7.2 Rectifying Contacts

When a forward-bias voltage V is applied to the Schottky barrier of Fig. 5-31b, the contact potential is reduced from V_0 to $V_0 - V$ (Fig. 5-33a). As a result, electrons in the semiconductor conduction band can diffuse across the depletion region to the metal. This gives rise to a forward current (metal to semiconductor) through the junction. Conversely, a reverse bias increases the barrier to $V_0 + V_r$, and electron flow from semiconductor to metal becomes negligible. In either case flow of electrons from the metal to the semiconductor is retarded by the barrier $\Phi_m - \chi$. The resulting diode equation is similar in form to that of the p-n junction

$$I = I_0(e^{qV/kT} - 1) \tag{5-76}$$

as Fig. 5-33c suggests. In this case the reverse saturation current I_0 is not simply derived as it was for the p-n junction. One important feature we can predict intuitively, however, is that the saturation current should depend upon the size

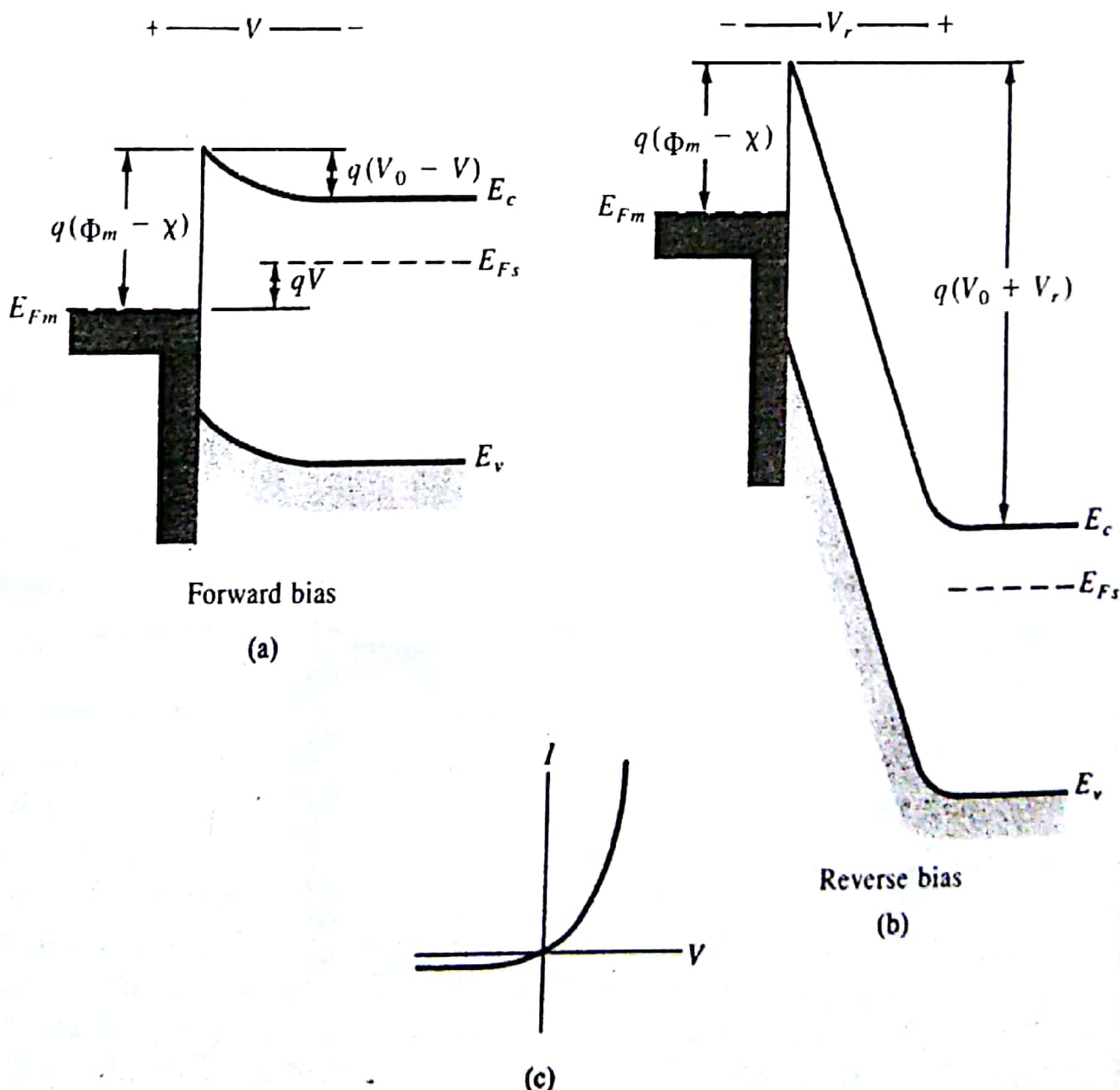

Figure 5-33 Effects of forward and reverse bias on the junction of Fig. 5-31: (a) forward bias; (b) reverse bias; (c) typical current–voltage characteristic.

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of the barrier Φ_B for electron injection from the metal into the semiconductor. This barrier (which is $\Phi_m - \chi$ for the ideal case shown in Fig. 5-33) is unaffected by the bias voltage. We expect the probability of an electron in the metal surmounting this barrier to be given by a Boltzmann factor. Thus

$$I_0 \propto e^{-q\Phi_B/kT} \tag{5-77}$$

The diode equation (5-76) applies also to the metal–p-type semiconductor junction of Fig. 5-32. In this case forward voltage is defined with the semiconductor biased positively with respect to the metal. Forward current increases as this voltage lowers the potential barrier to $V_0 - V$ and holes flow from the semiconductor to the metal. Of course, a reverse voltage increases the barrier for hole flow and the current becomes negligible.

In both of these cases the Schottky barrier diode is rectifying, with easy current flow in the forward direction and little current in the reverse direction. We also note that the forward current in each case is due to the injection of *majority* carriers from the semiconductor into the metal. The absence of minority carrier injection and the associated storage delay time is an important feature of Schottky barrier diodes. Although some minority carrier injection occurs at high current levels, these are essentially majority carrier devices. Their high-frequency properties and switching speed are therefore generally better than typical p-n junctions.

In the early days of semiconductor technology, rectifying contacts were made simply by pressing a wire against the surface of the semiconductor. In modern devices, however, the metal–semiconductor contact is made by depositing an appropriate metal film on a clean semiconductor surface and defining the contact pattern photolithographically. Schottky barrier devices are particularly well suited for use in densely packed integrated circuits, because fewer photolithographic masking steps are required compared to p-n junction devices.

5.7.3 Ohmic Contacts

In many cases we wish to have an *ohmic* metal–semiconductor contact, having a linear *I–V* characteristic in both biasing directions. For example, the surface of a typical integrated circuit is a maze of p and n regions, which must be contacted and interconnected. It is important that such contacts be ohmic, with minimal resistance and no tendency to rectify signals.

Ideal metal–semiconductor contacts are ohmic when the charge induced in the semiconductor in aligning the Fermi levels is provided by majority carriers (Fig. 5-34). For example, in the $\Phi_m < \Phi_s$ (n-type) case of Fig. 5-34a, the Fermi levels are aligned at equilibrium by transferring electrons from the metal to the semiconductor. This raises the semiconductor electron energies (lowers the electrostatic potential) relative to the metal at equilibrium (Fig. 5-34b). In this case the barrier to electron flow between the metal and the semiconductor is small and easily overcome by a small voltage. Similarly, the case $\Phi_m > \Phi_s$ (p-type) results in easy hole flow across the junction (Fig. 5-34d). Unlike the

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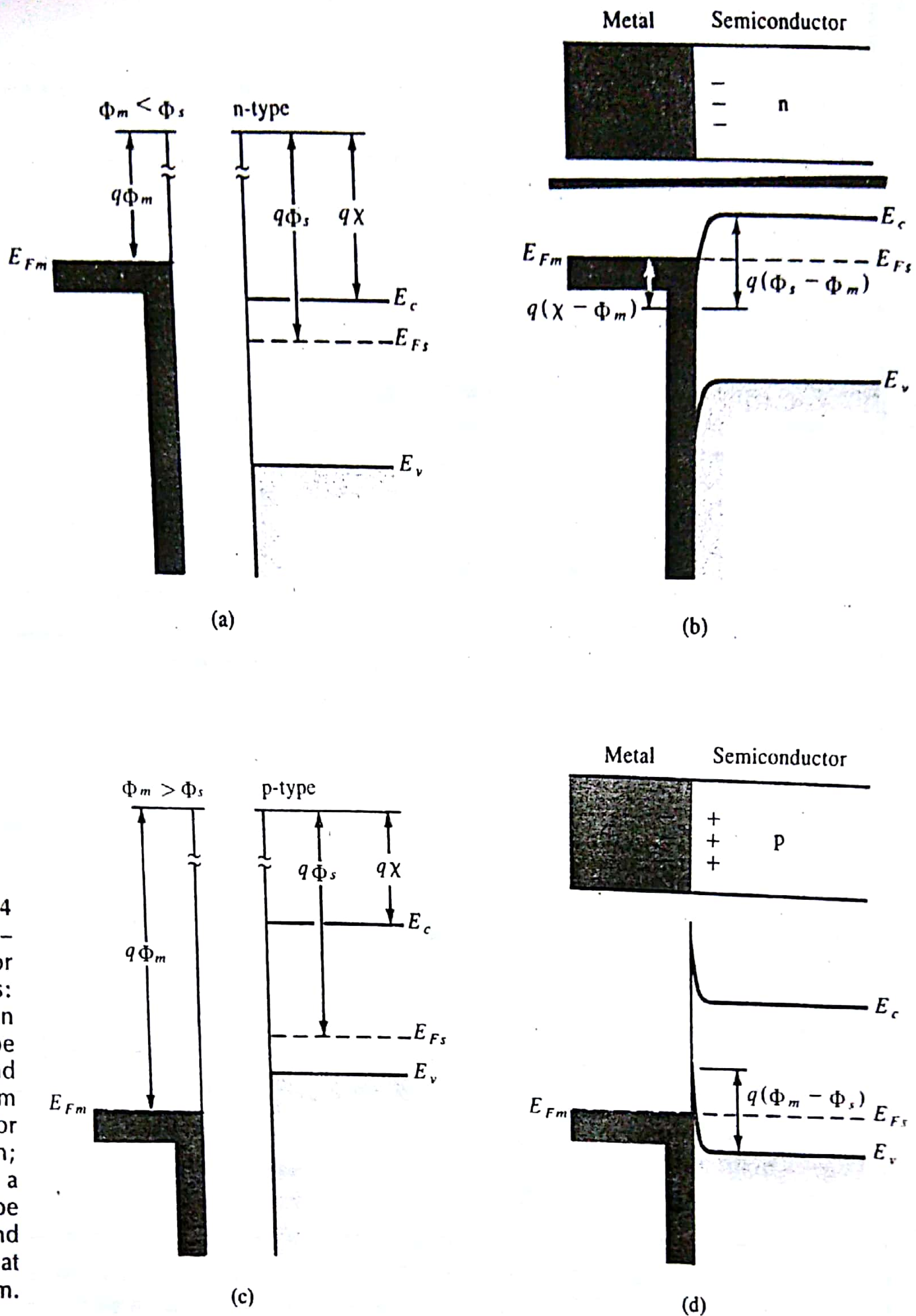

Figure 5-34 Ohmic metal–semiconductor contacts: (a) $\Phi_m < \Phi_s$ for an n-type semiconductor, and (b) the equilibrium band diagram for the junction; (c) $\Phi_m > \Phi_s$ for a p-type semiconductor, and (d) the junction at equilibrium.

rectifying contacts discussed above, no depletion region occurs in the semiconductor in these cases since the electrostatic potential difference required to align the Fermi levels at equilibrium calls for accumulation of majority carriers in the semiconductor.

A practical method for forming ohmic contacts is by doping the semiconductor heavily in the contact region. Thus if a barrier exists at the interface, the depletion width is small enough to allow carriers to tunnel through the barrier. For example, Au containing a small percentage of Sb can be alloyed to n-type

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Si, forming an n^+ layer at the semiconductor surface and an excellent ohmic contact. Similarly, p-type material requires a p^+ surface layer in contact with the metal. In the case of Al on p-type Si, the metal contact also provides the acceptor dopant. Thus the required p^+ surface layer is formed during a brief heat treatment of the contact after the Al is deposited. As we shall see in the discussion of integrated circuits in Chapter 9, Al makes good ohmic contact to p-type Si, but n-type material requires an n^+ diffusion or implantation before contacting by Al.

5.7.4 Typical Schottky Barriers

The discussion of ideal metal–semiconductor contacts does not include certain effects of the junction between the two dissimilar materials. Unlike a p-n junction, which occurs within a single crystal, a Schottky barrier junction includes a termination of the semiconductor crystal. The semiconductor surface contains *surface states* due to incomplete covalent bonds and other effects, which can lead to charges at the metal–semiconductor interface. Furthermore, the contact is seldom an atomically sharp discontinuity between the semiconductor crystal and the metal. There is typically a thin interfacial layer, which is neither semiconductor nor metal. For example, silicon crystals are covered by a thin (10–20 Å) oxide layer even after etching or cleaving in atmospheric conditions. Therefore, deposition of a metal on such a Si surface leaves a glassy interfacial layer at the junction. Although electrons can tunnel through this thin layer, it does affect the barrier to current transport through the junction.

Because of surface states, the interfacial layer, microscopic clusters of metal–semiconductor phases, and other effects, it is difficult to fabricate junctions with barriers near the ideal values predicted from the work functions of the two isolated materials. Therefore, measured barrier heights are used in device design. In compound semiconductors the interfacial layer introduces states in the semiconductor band gap that pin the Fermi level at a fixed position, regardless of the metal used (Fig. 5-35). For example, a collection of interface

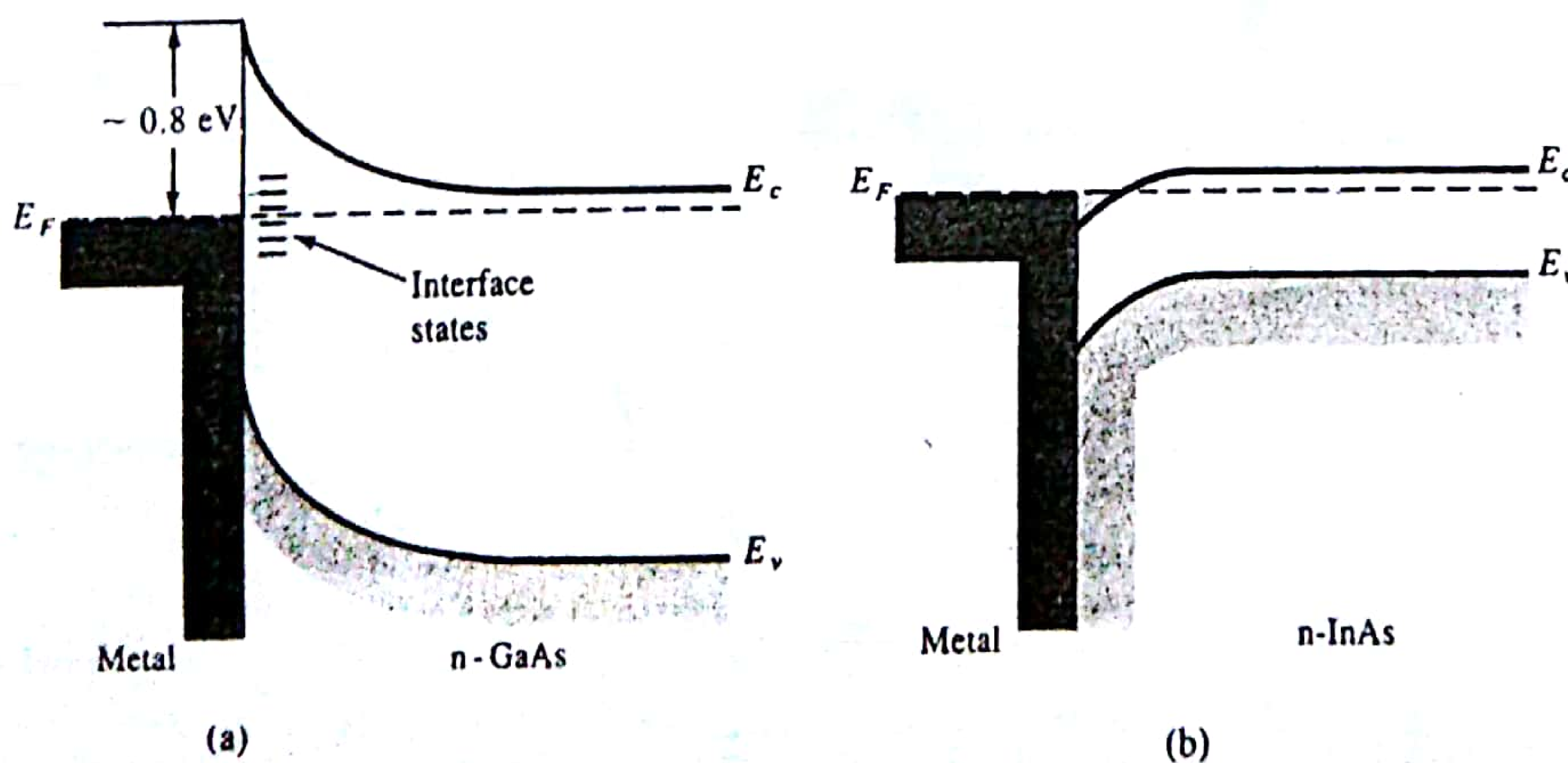

Figure 5-35 Fermi level pinning by interface states in compound semiconductors: (a) E_F is pinned near $E_C - 0.8$ eV in n-type GaAs, regardless of the choice of metal; (b) E_F is pinned above E_C in n-type InAs, providing an excellent ohmic contact.

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states located 0.7 ~ 0.9 eV below the conduction band pins E_F at the surface of n-type GaAs, and the Schottky barrier height is determined from this pinning effect rather than by the work function of the metal. An interesting case is n-type InAs (Fig. 5-35b), in which E_F at the interface is pinned *above* the conduction band edge. As a result, ohmic contact to n-type InAs can be made by depositing virtually any metal on the surface. For Si, good Schottky barriers are formed by various metals, such as Au or Pt. In the case of Pt, heat treatment results in a platinum silicide layer, which provides a reliable Schottky barrier with $\Phi_B \simeq 0.85$ V on n-type Si.

A full treatment of Schottky barrier diodes results in a forward current equation of the form

$$I = ABT^2 e^{-q\Phi_B/kT} e^{qV/\mathbf{n}kT} \tag{5-78}$$

where B is a constant containing parameters of the junction properties and $\mathbf{n}$ is a number between 1 and 2, similar to the ideality factor in Eq. (5-71) but arising from different reasons. The mathematics of this derivation is similar to that of *thermionic emission*, and the factor B corresponds to an effective Richardson constant in the thermionic problem.

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8.1.3 Varactor Diode and Parametric Amplifier

The term *varactor* is an abbreviation for variable capacitor. As noted in section 2.3.5, a reverse-biased pn-junction behaves like a parallel-plate capacitor the magnitude of which depends on the reverse bias :

$$C_T = \frac{C_{T0}}{(1 + V/V_d)^m} \tag{8.1.11}$$

where m depends on the type of the junction and V_d is the barrier potential. For reverse biases large compared to V_d we can write eqn. (8.1.11) in the form

$$C_T \propto V^{-m} \tag{8.1.12}$$

Let us consider a $p^+ - n$ junction so that the depletion region extends primarily into the n-side. Three common types of doping profiles are shown in Fig. 8.4. Donor distribution is assumed to be

$$N_D = ax^n \tag{8.1.13}$$

where a is a constant and the exponent $n = 0, 1,$ or $-\frac{3}{2}$ corresponds to abrupt, linearly graded, or hyperabrupt junction. It can be shown that

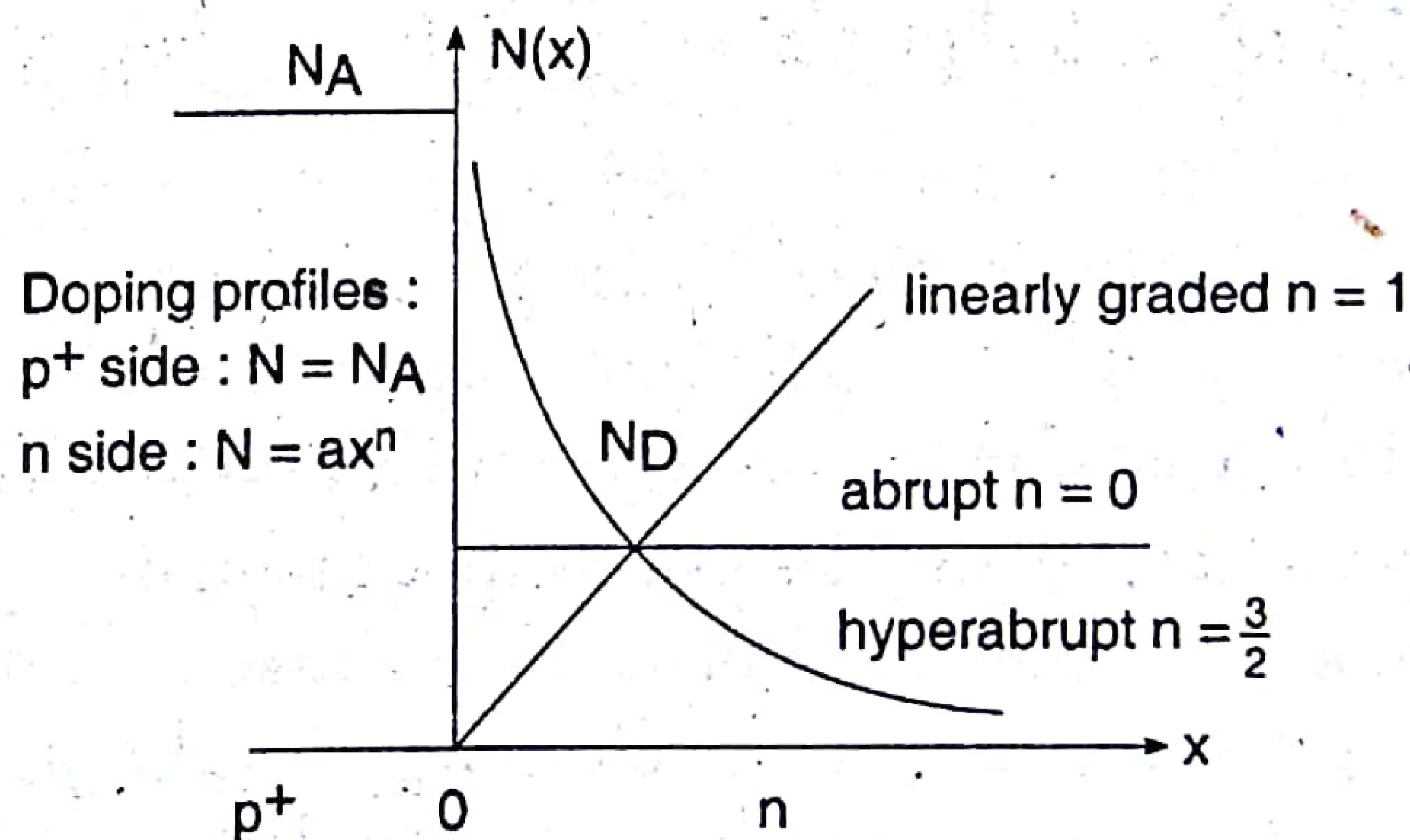

Fig. 8.4 Graded junction Profiles

$$m = \frac{1}{n+2} \tag{8.1.14}$$

for the $p^+ - n$ junction (or, for that matter, $n^+ - p$ junction). The hyperabrupt junction (which is true only for a short-distance away from the junction) is particularly interesting for certain varactor applications. In this case, $m = 2$ and according to eqn. (8.1.12) the capacitance will be proportional to V^{-2}. When such a varactor is used in a resonant circuit with inductance L, the resonant frequency will be

$$f = \frac{1}{2\pi\sqrt{LC_T}} \propto V \tag{8.1.15}$$

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Reversed-biased junction diodes are often used as small signal capacitors whose capacitance can be electrically controlled by their dc bias. Diodes especially made for this purpose are called *tuning diodes* or *varactors*. They are used for electronic tuning of high-freuqency resonant circuits to the desired frequency as needed, e.g., in selection of proper T.V. channel. Other important uses are in microwave amplification (parametric amplifiers) or generation (frequency multipliers).

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8.1.4 IMPATT Diode

A diode biased in the reverse direction, so that it operates in the avalanche region, can generate microwave frequencies. The word IMPATT stands for "*Impact-ionization Avalanche Transist Time*". These diodes employ impact-ionization and transit-time properties of semiconductor structures to produce negative resistance at microwave frequencies. The negative resistance arises from two delays which cause the current to lag behind the voltage. One is the *avalanche delay* caused by finite build-up time of the avalanche current; the other is the '*transit-time* delay from the finite time for the carriers to cross the drift region, as shown in Fig. 8.6(a). When these two delays add up to half-cycle time (i.e., 180° phase shift), the current decreases as the voltage increases; in other words, the diode electronic resistance is negative at the corresponding frequency.

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[1] A. van der Ziel, Solid State Physical Electronics, 2nd ed. Ch. 14, Prentice Hall India Pvt. Ltd., 1971

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This dynamic (or ac) negative differential resistance is used to generate microwave power, as in the case of tunnel diode. The IMPATT diode is now one of the most powerful solid-state sources of microwave power. At present, this diode can generate the highest continuous wave (cw) power output at *mm*-wave frequencies (i.e., above 30 GHz) of all solid state devices.

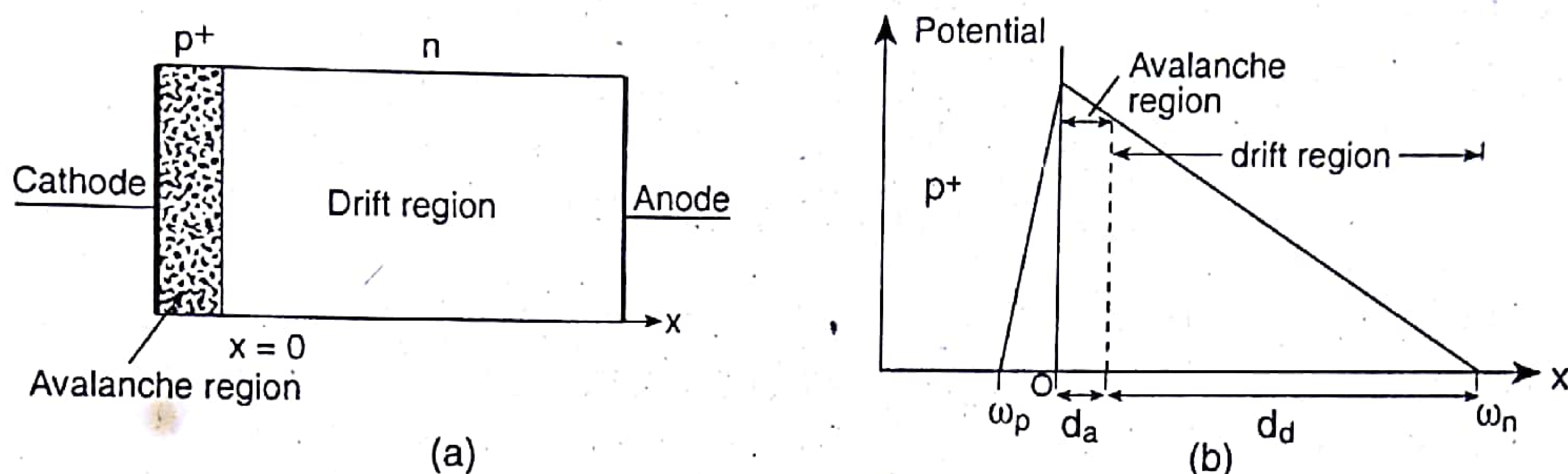

Fig. 8.6 IMPATT diode (a) Schematic diagram, (b) Potential distribution

Although detailed calculations of IMPATT operation are complicated and generally require computer solutions, the basic physical mechanism is simple. The structure of a $p^+ - n$ device is shown in Fig. 8.6(a). When a large enough reverse bias is applied to the device, carriers are generated by the avalanche break-down process in the high-field region (shown in Fig. 8.6(b)) at the $p^+ - n$ interface. These avalanche-generated carriers move in the electric field, not by diffusion but by drift, creating the electric current at the $p^+ - n$ interface. There is a relatively thin part of the space-charge region on the n-side of the junction, where avalanche multiplication occurs. In the remainder of the space-charge region the carriers drift but *do not multiply*. Because of the high fields involved, the drift velocity saturates. In other words, this drift will occur with the limiting drift velocity v_d for most of the space-charge region. Since the p-region of the junction is heavily doped, $N_A > N_D$, and consequently width of the space charge region in p-type material will be much less than that of the n-type material (eqn. 2.3.6), i.e., $\omega_p \ll \omega_n$, as shown in Fig. 8.6(b). Then the total impedance can be divided into three groups :

$$Z_{tot} = R_s + Z_a + Z_d$$

where Z_a and Z_d are the impedances of the avalanche and drift regions respectively, and R_s is the series resistance for the remaining part of the diode. If such a diode is subjected to a varying electric field

$$E(t) = E_0 + E_m e^{j\omega t}$$

that it can be shown that[2]

$$Z_{tot} = R_S + \frac{d_d^2}{2\varepsilon\varepsilon_0 A v_d} \cdot \frac{2(1-\cos\theta)/\theta^2}{1-\omega^2/\omega_a^2} + \frac{1}{j\omega C_d} \frac{1 - \frac{\sin\theta}{\theta} - \frac{\omega^2}{\omega_a^2}\left(1 + \frac{da}{d_d}\right)}{1 - \omega^2/\omega_a^2} \quad (8.1.26)$$

[2]A. van der Ziel, Solid State Physical Electronics, 2nd. ed. ch 17, Prentice Hall India Pvt. Ltd., 1971

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$$\approx R_S + \frac{d_d^2}{2\varepsilon\varepsilon_0 A v_d}(1 - \omega^2/\omega_a^2)^{-1} + \frac{1}{j\omega c}\frac{-\omega^2/\omega_a^2}{1 - \omega^2/\omega_a^2} \quad (8.1.27)$$

if the *transit angle* $\theta = \omega d_d / v_d$ is assumed to be small. In eqn. (8.1.27)

$$\omega_a = \frac{1}{\sqrt{L_a C_a}} = \sqrt{\frac{2\bar{\alpha}_a' v_d I_0}{\varepsilon\varepsilon_0 A}} \quad (8.1.28)$$

$$L_a = \frac{d_a / v_d}{2\bar{\alpha}_a' I_0}, \quad C_a = \frac{\varepsilon\varepsilon_0 A}{d_a} \quad (8.1.29)$$

$$C = \varepsilon\varepsilon_0 A / (d_a + d_d) \quad (8.1.30)$$

where A is the junction area, I_0 the dc current through the diode, and $\bar{\alpha}_a'$ is somehow related to the rate of ionization in the avalanche region. C is the net capacitance of the space-charge region.

It is seen from eqn. (8.1.27) that its second term is an *active resistance* (a resistance that depends on frequency) that is negative for $\omega > \omega_a$. The third term is a parallel resonant circuit which includes the diode capacitance C and shunt inductor. To make the diode oscillate, we must add a parallel inductance L_S to the equivalent circuit to tune it, as shown in Fig. 8.7.

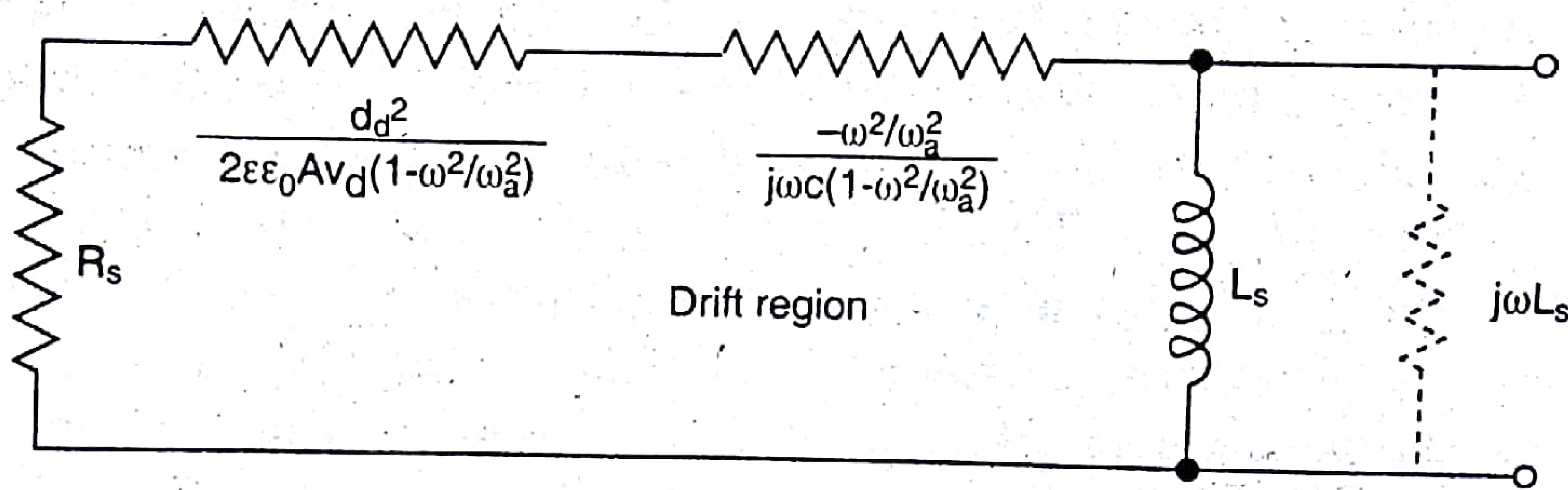

Fig. 8.7 Electrical analogue of IMPATT diode

It is interesting to note that strong negative resistance effects occur for relatively small transit angles. This negative resistance effect explains why the diode will oscillate for frequencies $\omega > \omega_a$.

From the discussion above it is understandable that avalanche diodes will oscillate at microwave frequencies and that the oscillator is current-tunable and tunable by external means. Powers of the order of 100 mW cW at 2GHz are obtainable. However, the obtainable power decreases with increasing frequency, and frequencies above 50 GHz have been generated. Pulsed operation results in much higher output power, of the order of 100 watts at 2GHz.

It has been seen that the peak value of negative resistance occurs near $\theta \gtrsim \pi$. For pactical purpose IMPATT diode works only in a frequency range around π transit angle, i.e.,

$$\theta = \pi = \omega\tau_d \text{ or, } f = \frac{1}{2\tau_d} = \frac{v_d}{2d_d} \quad (8.1.31)$$

For $v_d \sim 10^7$ cm/sec and $d_d \sim 10^{-5}$ cm, this comes around 100 GHz.

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