


[FET (Field Effect Transistor)]

DR. TILAK NARAYAN GHOSH
HOD, DEPARTMENT OF ELECTRONICS, MIDNAPORE COLLEGE (AUTONOMOUS)


Syllabus: Field Effect Transistors: JFET, Construction, Idea of Channel Formation, Pinch-Off and Saturation Voltage, Current-Voltage Output Characteristics. MOSFET, types of MOSFETs, Circuit symbols, Working and Characteristic curves of Depletion type MOSFET (both N channel and P Channel) and Enhancement type MOSFET (both N channel and P channel). Complimentary MOS (CMOS).

Introduction

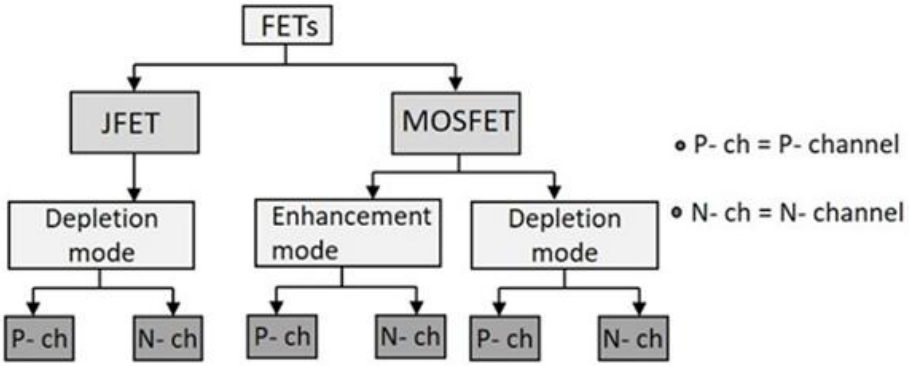
We know about ordinary transistor. In this type of transistor, both holes and electrons play part in the conduction process. For this reason, it is sometimes called a bipolar transistor. The ordinary or bipolar transistor has two principal disadvantages. First, it has a low input impedance because of forward biased emitter junction. Secondly, it has considerable noise level. Although low input impedance problem may be improved by careful design and use of more than one transistor, yet it is difficult to achieve input impedance more than a few megaohms. The field effect transistor (FET) has, by virtue of its construction and biasing, large input impedance which may be more than 100 megaohms. The FET is generally much less noisy than the ordinary or bipolar transistor. The rapidly expanding FET market has led many semiconductor marketing managers to believe that this device will soon become the most important electronic device, primarily because of its integrated-circuit applications. In this chapter, we shall focus our attention on the construction, working and circuit applications of field effect transistors.

Types of Field Effect Transistors

A bipolar junction transistor (BJT) is a current controlled device i.e., output characteristics of the device are controlled by base current and not by base voltage. However, in a field effect transistor (FET), the output characteristics are controlled by input voltage (i.e., electric field) and not by input current. This is probably the biggest difference between BJT and FET. There are two basic types of field effect transistors:

(i) Junction field effect transistor (JFET)

(ii) Metal oxide semiconductor field effect transistor (MOSFET) To begin with, we shall study about JFET and then improved form of JFET, namely; MOSFET



Characteristics of FET

I. FETs have high input impedance.
II. These devices are used in controlled switching between conducting and non-conducting states in digital circuits.
III. FETs are thermally stable.

Applications of FET

FET is used in circuits to reduce the loading effect.

FETs are used in many circuits such as Buffer Amplifier, Phase shift Oscillators and Voltmeters.

Comparison Between FET and BJT

Some of the general characteristics of FETs and BJT are compared below :

1. One of the most important characteristics of the FET is that it is simpler to fabricate and occupies less space on an IC chip than does a BJT. As a result the component density in FET IC can be extremely high.
2. A second important feature is that the input impedance of the FET is very high compared to that of a BJT.
3. The operation of a FET depends upon the flow of only one type of (majority) carrier. It is, therefore, a unipolar device in contrast to the BJT which is a bipolar device. In FET carriers are transported by drift process whereas in BJT the carriers move by the process of diffusion through the base.
4. The operation of a FET depends on the control of device current by the applied electric field. Thus the FET is voltage-controlled device whereas the BJT is basically a current controlled device.
5. The FET is less noisy than the BJT.
6. The temperature dependence of FET is usually smaller than that of BJT.
7. FET has the ability to dissipate high power and switch large currents at a faster rate than that achievable using BJT.
8. FET has higher switching speed and can be operated at higher frequencies. This is so because there is no minority carriers in FET. It can switch off faster since no storage charge has to be removed from the junction area.
9. The main *disadvantage* of the FET is the relatively low gain bandwidth product compared with that which can be obtained with the BJT. In some cases FETs become very susceptible to overload voltages and may require special handling during installation.

Junction Field-Effect Transistor (JFET)

Structure

The basic structure of an n-channel JFET is shown in Fig. 1. It consists of a uniformly doped n-type semiconductor bar with two ohmic contacts at its two ends. Current is caused to flow through the bar by applying a voltage between the end terminals. The terminal through which the majority carriers (here electrons) enter the bar is called the *source*. The other terminal through which the majority carriers leave the bar is called the *drain*. On two sides of the n-type bar p-n junctions are formed by doping the sides heavily with p-type impurities. These impurity regions are called the *gate*. The region of the n-type bar between the two gate regions through which majority carriers move from source to drain is called the *channel*. The circuit symbol of an n-channel JFET is shown in Fig -1(b), where the arrow head is in the direction of conventional current when the gate is forward biased.

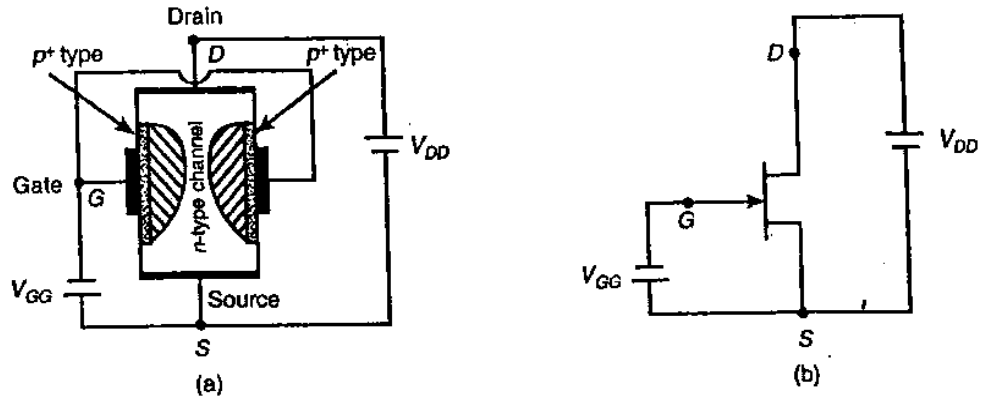


Fig.-1: An n-channel JFET (a) Structure (b) Circuit symbol with supply voltages

A p-channel JFET consists of a p-type semiconductor bar with two ohmic contacts at its two ends. As before one of them is the source through which majority carriers enter the bar. The other terminal is the drain through which majority holes leave the bar. The two sides of the p-type bar are doped heavily with n-type impurities. These regions are called the *gate*. The region of p-type bar between the two gate regions through which majority carriers move from source to drain is called the channel. The structure and the circuit symbol of p-channel JFET are shown in Fig. 2.

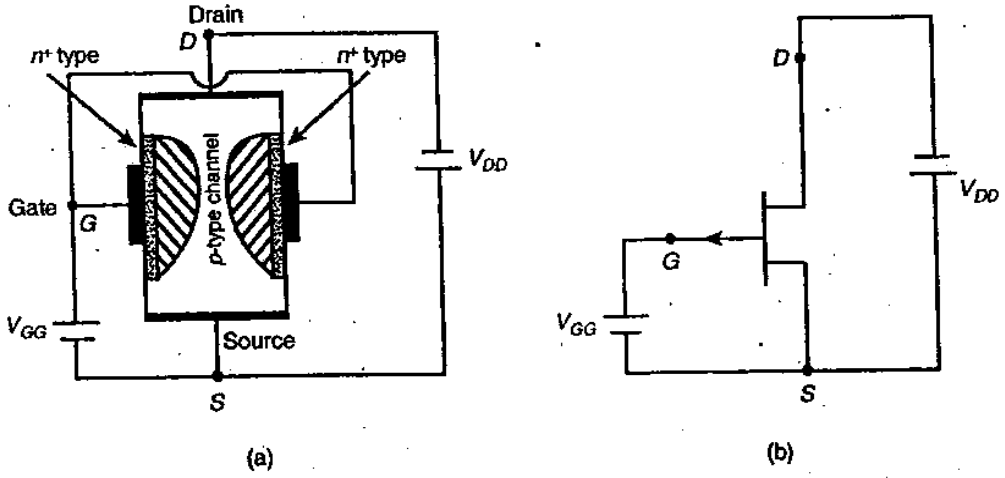


Fig.-2: p-channel JFET (a) Structure (b) Circuit symbol with supply voltages

Operation of n-channel JFET

To understand the principle of operation of a JFET, let us consider an *n*-channel JFET connected in common source mode with the gate junction reverse-biased. On two sides of the reverse-biased *p-n* junction, depletion regions are formed. Since the gate *p*-region is heavily doped the depletion layer extends mainly into the channel *n*-region (Fig. 9.3-1). When a current passes through the channel between source and drain there is gradual ohmic potential drop across the channel. This makes the gate more reverse biased near the drain end than the source end. As a result width of the depletion region becomes more near the drain end than the source end of the gate. This makes the drain current to flow through an effectively wedge-shaped channel because there is no mobile charges in the depletion region. Now if the gate reverse-bias voltage is increased the depletion region extends further into the channel region and hence the effective channel cross-section for current flow decreases. It decreases channel conductance and drain current. Thus the transverse electric field introduced by the gate is used to control the device current and this is why the device is called a field-effect transistor.

The above explanation applies equally to the *p*-channel JFET, the only difference is that voltage polarities are to be reversed and the role of electron and hole interchanged.

Static Characteristics of n-channel JFET

The gate-source junction is reversed biased. For n-channel JFET , the electron drift from source to drain, thus current flows from drain to source which is called drain current (I_D).

The graphical plots of the drain current (I_D) against drain to source voltage (V_{DS}) with the gate to source voltage (V_{GS}) as a parameter are known as *Static Characteristics* of a JFET.

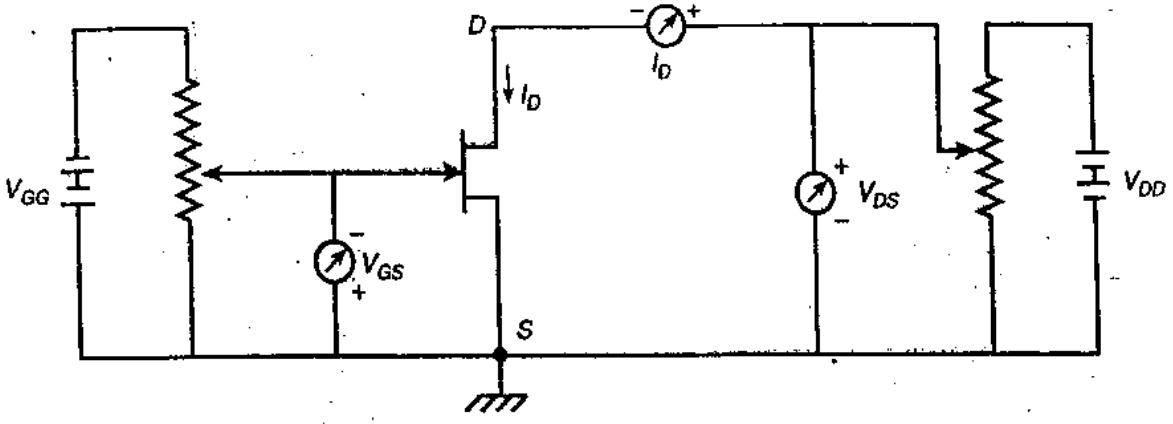


Fig.3: Circuit arrangement for drawing the characteristic curves of an *n* channel JFET (for a *p*-channel JFET just reverse the polarities of the batteries and the meters)

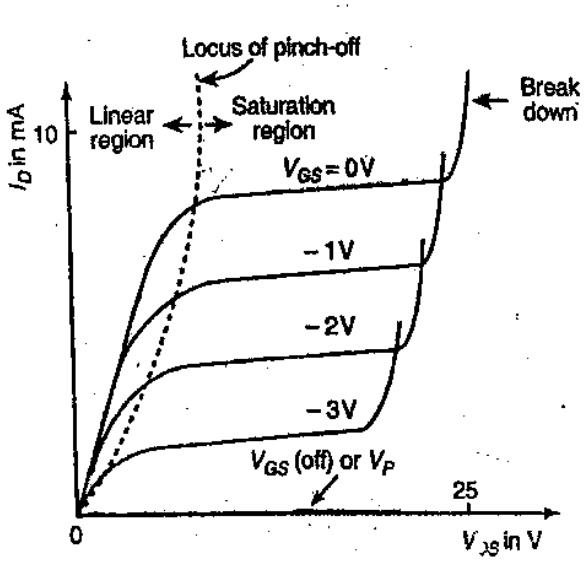


Fig.4: Drain characteristics of typical *n*-channel JFET

Fig. 4 shows the drain characteristics for a typical *n*-channel JFET. Each of characteristic curves can be divided into there regions: (i) the ohmic or *linear region* where I_D is approximately proportional to V_{DS} (ii) *the saturation region* where I_D is almost constant and independent of V_{DS} and (iii) the *breakdown region* where I_D rises abruptly to large values. To explain the nature of the curves we first consider the curve with $V_{GS} = 0$.

- **The linear or ohmic region -**

We consider V_{GS}=0; when a positive voltage V_{DS} is applied to the drain w.r.to V_x along the channel increases from small value, the width of the depletion regions remain very small and the conductor bar behaves as a simple resistor. Thus I_D (drain current) increases linearly with $V_{DS.}$ This region is known as linear region.

- **Saturation region –**

When V_{GS}=0; then reverse bias across each point in the gate channel is V_x and reverse bias is relatively large near the drain and decreases gradually towards the source. As V_{DS} is solely increased the depletion layer widths increase constricting the channel opening. As V_{DS} continues to increase, the channel opening near the drain shrinks and channel resistances increases further. At some value V_{DS} the depletion regions meet near the drain to pinch off the channel. This value V_{DS} is called saturation voltage V_{DSAT} . Beyond pinch-off the current I_D saturates at a value I_{DSAT} .

- **Breakdown region –**

For a large value of V_{DS} ,the reverse voltage between the channel and the gate becomes sufficient to causes a breakdown of the gate junction, resulting in a sharp increase of the drain current.

When V_{GS} is negative the channel resistance increases because of reverse bias between the channel and the gate . Hence I_D is reduced for a given V_{DS} and pinch-off occours at a lower value of V_{DS} .Breakdown also takes place at lower value of V_{DS} as V_{DS} and V_{DS} contribute to the breakdown voltage.

Define "pinch off" voltage of a JFET. Sketch the depletion region before and after pinch-off

From the drain characteristics of Fig. 4 it is found that in the saturation region I_D decreases with increase in reverse bias gate source voltage. Practically for certain value of V_{GS} the drain current is reduced to zero. This voltage is called *gate-source cut off voltage* or pinch off voltage and is labelled as V_{GS}(off) or V_P. At this voltage the conducting channel disappears. Note that V_P is negative for n-channel device and positive for p-channel device.

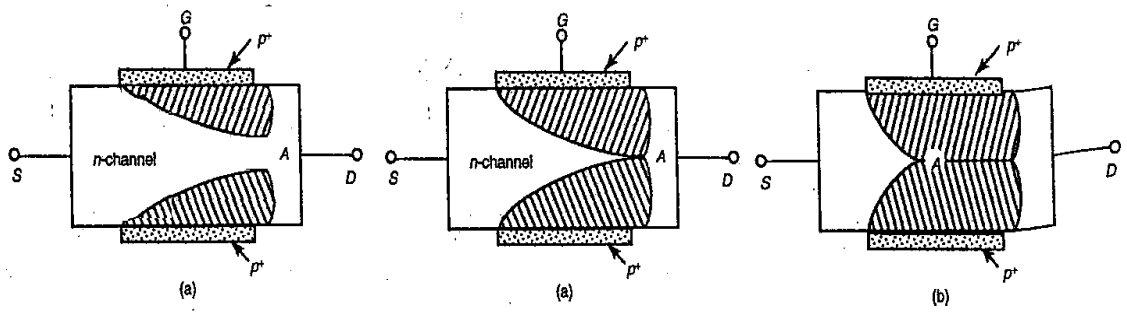


Fig. 5 : Channel of JFET (a) before pinch-off (b) at pinch-off (b) beyond pinch-off

Expression for Drain Current (I_D)

The relation between I_{DSS} and V_p is shown in Fig. 6 We note that gate-source cut off voltage [*i.e.* $V_{GS\,(off)}$] on the transfer characteristic is equal to pinch off voltage V_p on the drain characteristic *i.e.*

$$V_P = |V_{GS\,(off)}|$$

For example, if a *JFET* has $V_{GS\,(off)} = -4$V, then $V_P = 4$V.

The transfer characteristic of *JFET* shown in Fig. 6 is part of a parabola. A rather complex mathematical analysis yields the following expression for drain current :

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS\,(off)}}\right]^2$$

where

I_D = drain current at given V_{GS}

I_{DSS} = shorted – gate drain current

V_{GS} = gate–source voltage

$V_{GS\,(off)}$ = gate–source cut off voltage

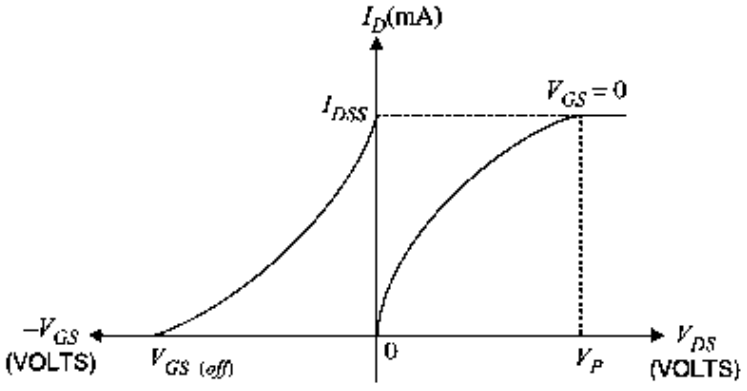
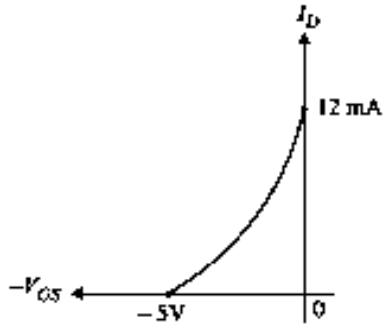


Fig 6

Example 1. *Fig. shows the transfer characteristic curve of a JFET. Write the equation for drain current.*



Solution. Referring to the transfer characteristic curve in Fig. we have,

$$I_{DSS} = 12 \text{ mA}$$

$$V_{GS(off)} = -5 \text{ V}$$

$$\therefore \quad I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

$$\text{or} \quad I_D = 12\left[1 + \frac{V_{GS}}{5}\right]^2 \text{ mA. Ans.}$$

Example 2. *A JFET has the following parameters: $I_{DSS} = 32$ mA ; $V_{GS(off)} = -8V$; $V_{GS} = -4.5$ V. Find the value of drain current.*

Solution.

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

$$= 32\left[1 - \frac{(-4.5)}{-8}\right]^2 \text{ mA}$$

$$= 6.12 \text{ mA}$$

Example 3. *A JFET has a drain current of 5 mA. If $I_{DSS} = 10$ mA and $V_{GS(off)} = -6$ V, find the value of (i) V_{GS} and (ii) V_P*

Solution.

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

or

$$5 = 10\left[1 + \frac{V_{GS}}{6}\right]^2$$

or

$$1 + \frac{V_{GS}}{6} = \sqrt{5/10} = 0.707$$

(i) $\therefore \quad V_{GS} = -1.76$ V

(ii) and $\quad V_P = -V_{GS(off)} = 6$ V

Example 4. *For the JFET in Fig. $V_{GS(off)} = -4V$ and $I_{DSS} = 12$ mA. Determine the minimum value of V_{DD} required to put the device in the constant-current region of operation.*

Solution. Since $V_{GS(off)} = -4$V, $V_P = 4$V. The minimum value of V_{DS} for the *JFET* to be in constant-current region is

$$V_{DS} = V_P = 4\text{V}$$

In the constant current region with $V_{GS} = 0$V,

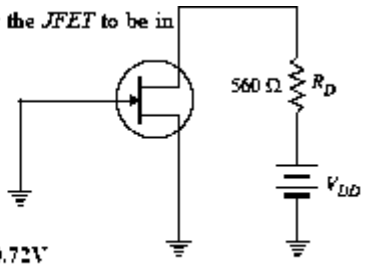
$$I_D = I_{DSS} = 12 \text{ mA}$$

Applying Kirchhoff's voltage law around the drain circuit, we have,

$$V_{DD} = V_{DS} + V_{R_D} = V_{DS} + I_D R_D$$

$$= 4\text{V} + (12 \text{ mA})(560\Omega) = 4\text{V} + 6.72\text{V} = 10.72\text{V}$$

This is the value of V_{DD} to make $V_{DS} = V_P$ and put the device in the constant-current region.



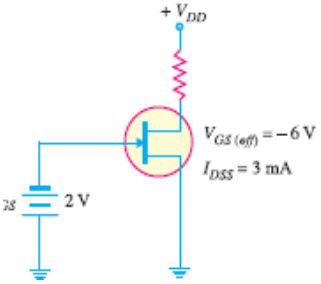
Example 5. *Determine the value of drain current for the circuit shown in Fig.*

Solution. It is clear from Fig. that $V_{GS} = -2$V. The drain current for the circuit is given by;

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

$$= 3 \text{ mA}\left(1 - \frac{-2\text{V}}{-6\text{V}}\right)^2$$

$$= (3 \text{ mA})(0.444) = 1.33 \text{ mA}$$



Advantages of JFET

A *JFET* is a voltage controlled, constant current device (similar to a vacuum pentode) in which variations in input voltage control the output current. It combines the many advantages of both bipolar transistor and vacuum pentode. Some of the advantages of a *JFET* are :

(*i*) It has a very high input impedance (of the order of 100 MΩ). This permits high degree of isolation between the input and output circuits.

(*ii*) The operation of a *JFET* depends upon the bulk material current carriers that do not cross junctions. Therefore, the inherent noise of tubes (due to high-temperature operation) and those of transistors (due to junction transitions) are not present in a *JFET*.

(*iii*) A *JFET* has a negative temperature co-efficient of resistance. This avoids the risk of thermal runaway.

(*iv*) A *JFET* has a very high power gain. This eliminates the necessity of using driver stages.

(*v*) A *JFET* has a smaller size, longer life and high efficiency.

JFET Parameters

The analytical method of analysis of JFET amplifiers involves three parameters, called JFET parameters. These are determined by the slopes of the characteristic curves. These are defined below :

1. **Drain resistance r_d :** It is the a.c. resistance between drain and source terminals and is defined as the ratio of the small change in drain voltage to the corresponding change in drain current at a constant gate voltage i.e.,

$$r_d = \frac{\delta V_{DS}}{\delta I_D}\Big|_{V_{GS}=\text{constant}} \qquad (1)$$

2. **Mutual conductance g_m :** It is defined as ratio of small change in drain current to the corresponding change in the gate voltage at a constant drain voltage, i.e.,

$$g_m = \frac{\delta I_D}{\delta V_{GS}}\Big|_{V_{DS}=\text{constant}} \qquad (2)$$

3. **Amplification factor μ :** It is defined as the small change in drain voltage to the corresponding change in gate voltage for a constant drain current, i.e.,

$$\mu = -\frac{\delta V_{DS}}{\delta V_{GS}}\Big|_{I_D=\text{constant}} \qquad (3)$$

where the negative sign indicates that any change in I_D due to a positive increment of V_{DS} is to be counterbalanced by a negative increment of V_{GS}. Physically μ represents the relative effectiveness of the gate voltage over the drain voltage in controlling the drain current.

Relation between μ, r_d and g_m.

The drain current I_D is a function of drain voltage V_{DS} and gate voltage V_{GS} i.e.,

$$I_D = f(V_{DS}, V_{GS})$$

$$\therefore \quad dI_D = \frac{\partial I_D}{\partial V_{DS}}\Big|_{V_{GS}} dV_{DS} + \frac{\partial I_D}{\partial V_{GS}}\Big|_{V_{DS}} .dV_{GS}$$

If V_{DS} and V_{GS} are simultaneously so changed that I_D remains constant then $dI_D = 0$ and we can write from Eq. (9.5-4) after rearrangement,

$$\frac{\partial I_D}{\partial V_{DS}}\Big|_{V_{GS}} \cdot \frac{\partial V_{DS}}{\partial V_{GS}}\Big|_{I_D} + \frac{\partial I_D}{\partial V_{GS}}\Big|_{V_{DS}} = 0$$

Now using the definitions (1)-(3),

$$\frac{1}{r_d}(-\mu) + g_m = 0$$

$$\text{or,} \quad \mu = r_d \cdot g_m \qquad (5)$$

Variation of Transconductance (g_m) of JFET

We have seen that transconductance gm of a JFET is the ratio of a change in drain current (Δ_{ID}) to a change in gate-source voltage (ΔV_{GS}) at constant V_{DS} i.e.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

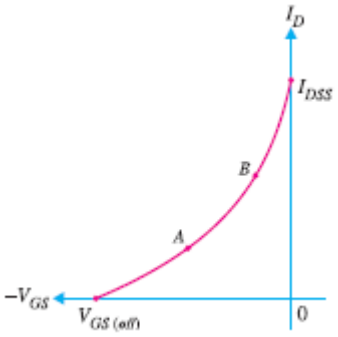


Fig 7

The transconductance g_m of a JFET is an important parameter because it is a major factor in determining the voltage gain of JFET amplifiers. However, the transfer characteristic curve for a JFET is nonlinear so that the value of g_m depends upon the location on the curve. Thus the value of gm at point A in Fig.7 will be different from that at point B. Luckily, there is following equation to determine the value of gm at a specified value of V_{GS} :

$$g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_{GS}(off)}\right)$$

where g_m = value of transconductance at any point on the transfer characteristic curve

g_{mo} = value of transconductance(maximum) at $V_{GS} = 0$

Normally, the data sheet provides the value of g_{mo}. When the value of g_{mo} is not available, you can approximately calculate g_{mo} using the following relation :

$$g_{mo} = \frac{2I_{DSS}}{|V_{GS}(off)|}$$

Metal Oxide Semiconductor FET (MOSFET)

The main drawback of *JFET* is that its gate *must* be reverse biased for proper operation of the device *i.e.* it can only have negative gate operation for *n*-channel and positive gate operation for *p*-channel. This means that we can *only* decrease the width of the channel (*i.e.* decrease the conductivity of the channel) from its zero-bias size. This type of operation is referred to as *depletion-mode* operation. Therefore, a *JFET* can only be operated in the depletion-mode. However, there is a field effect transistor (*FET*) that can be operated to enhance (or increase) the width of the channel (with consequent increase in conductivity of the channel) *i.e.* it can have *enhancement-mode* operation. Such a *FET* is called *MOSFET*.

A field effect transistor (FET) that can be operated in the enhancement-mode is called a ***MOSFET****.*

A *MOSFET* is an important semiconductor device and can be used in any of the circuits covered for *JFET*. However, a *MOSFET* has several advantages over *JFET* including high input impedance and low cost of production.

Types of MOSFETs

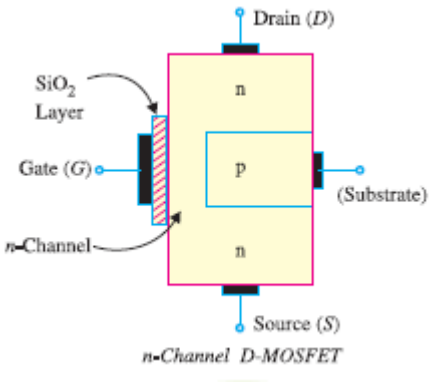
There are two basic types of *MOSFETs viz.*

1. Depletion-type *MOSFET* or ***D-MOSFET.*** The *D-MOSFET* can be operated in both the depletion-mode and the enhancement-mode. For this reason, a *D-MOSFET* is sometimes called depletion/enhancement *MOSFET*.

2. Enhancement-type *MOSFET* or ***E-MOSFET.*** The *E-MOSFET* can be operated *only* in enhancement- mode. The manner in which a *MOSFET* is constructed determines whether it is *D-MOSFET* or *EMOSFET*.

1. D-MOSFET. Fig. shows the constructional details of *n*-channel *D-MOSFET*. It is similar to *n*-channel *JFET* except with the following modifications/remarks :

(*i*) The *n*-channel *D-MOSFET* is a piece of *n*-type material with a *p*-type region (called *substrate*) on the right and an *insulated gate* on the left as shown in Fig.. The free electrons (Q it is *n*-channel) flowing from source to drain must pass through the narrow channel between the gate and the *p*-type region (*i.e.* substrate).



n-Channel D-MOSFET

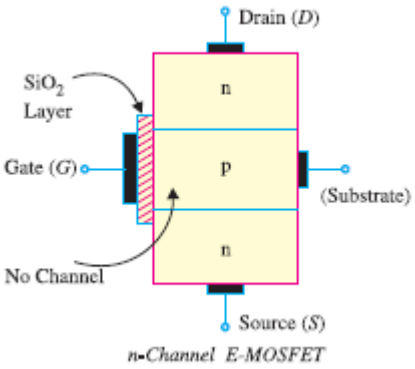
(*ii*) Note carefully the gate construction of *D-MOSFET*. A thin layer of metal oxide (usually silicon dioxide, SiO_2) is deposited over a small portion of the channel. A metallic gate is deposited over the oxide layer. As SiO_2 is an insulator, therefore, gate is insulated from the channel. Note that the arrangement forms a capacitor.

One plate of this capacitor is the gate and the other plate is the channel with SiO_2 as the dielectric. Recall that we have a gate diode in a *JFET*.

(*iii*) It is a usual practice to connect the substrate to the source (*S*) internally so that a *MOSFET* has three terminals *viz* *source* (*S*), *gate* (*G*) and *drain* (*D*).

(*iv*) Since the gate is insulated from the channel, we can apply either negative or positive voltage to the gate. Therefore, *D-MOSFET* can be operated in both depletion-mode and enhancement-mode. However, *JFET* can be operated only in depletion-mode.

E-MOSFET. Fig. shows the constructional details of *n*-channel *E-MOSFET*. Its gate construction is similar to that of *D-MOSFET*. The *E-MOSFET* has no channel between source and drain unlike the *D-MOSFET*. Note that the substrate extends completely to the SiO_2 layer so that no channel exists. The *E-MOSFET* requires a proper gate voltage to *form* a channel (called induced channel). It is reminded that *E-MOSFET* can be operated *only* in enhancement mode. In short, the construction of *E-MOSFET* is quite similar to that of the *D-MOSFET* except for the absence of a channel between the drain and source terminals.



n-Channel E-MOSFET

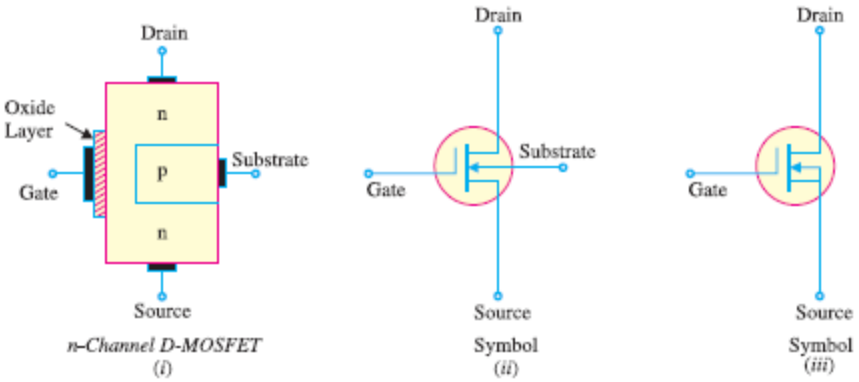
Why the name MOSFET ? The reader may wonder why is the device called *MOSFET?* The answer is simple. The SiO2 layer is an insulator. The gate terminal is made of a metal conductor. Thus, going from gate to substrate, you have a *metal oxide semiconductor* and hence the name *MOSFET*. Since the gate is insulated from the channel, the *MOSFET* is sometimes called *insulated-gate FET (IGFET)*. However, this term is rarely used in place of the term *MOSFET*.

Symbols for D-MOSFET

There are two types of *D-MOSFETs viz* (*i*) *n*-channel *D-MOSFET* and (*ii*) *p*-channel *D-MOSFET*.

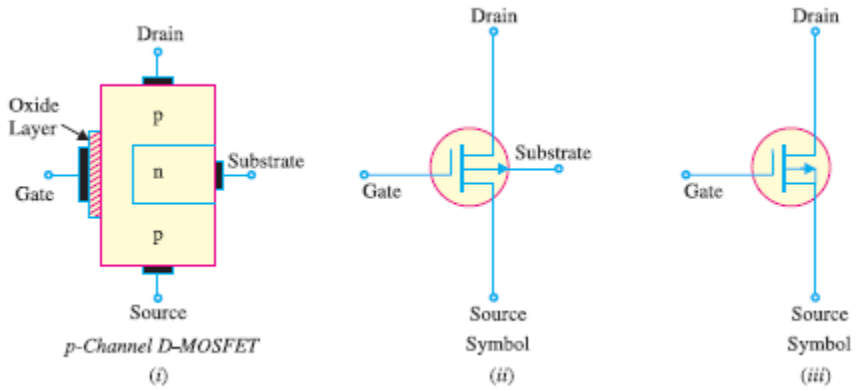
(*i*) n-channel D-MOSFET. Fig. 19.45 (*i*) shows the various parts of *n*-channel *D-MOSFET*.

The *p*-type substrate constricts the channel between the source and drain so that only a small passage remains at the left side. Electrons flowing from source (when drain is positive w.r.t. source) must pass through this narrow channel. The symbol for *n*-channel *D-MOSFET* is shown in Fig. (*ii*). The gate appears like a capacitor plate. Just to the right of the gate is a thick vertical line representing the channel. The drain lead comes out of the top of the channel and the source lead connects to the bottom. The arrow is on the substrate and points to the *n*-material, therefore we have *n*-channel *DMOSFET*.



It is a usual practice to connect the substrate to source internally as shown in Fig. 19.45 (*iii*). This gives rise to a three-terminal device.

(*ii*) *p*-channel D-MOSFET. Fig. (*i*) shows the various parts of *p*-channel *D-MOSFET*.

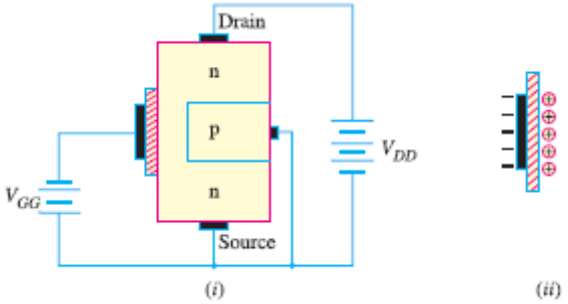


The *n*-type substrate constricts the channel between the source and drain so that only a small passage remains at the left side. The conduction takes place by the flow of holes from source to drain through this narrow channel. The symbol for *p*-channel *D-MOSFET* is shown in Fig. 19.46 (*ii*). It is a usual practice to connect the substrate to source internally. This results in a three-terminal device whose schematic symbol is shown in Fig. 19.46 (*iii*).

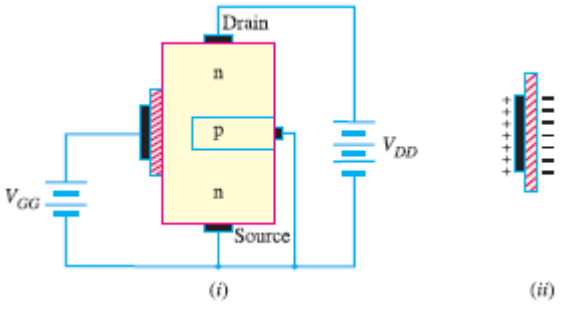
Circuit Operation of D-MOSFET

Fig. (*i*) shows the circuit of *n*-channel *D-MOSFET*. The gate forms a small capacitor. One plate of this capacitor is the gate and the other plate is the channel with metal oxide layer as the dielectric. When gate voltage is changed, the electric field of the capacitor changes which in turn changes the resistance of the n-channel. Since the gate is insulated from the channel, we can apply either negative or positive voltage to the gate. The negative-gate operation is called *depletion mode* whereas positive- gate operation is known as *enhancement mode.*

(*i*) Depletion mode. Fig. (*i*) shows depletion-mode operation of *n*-channel *D-MOSFET*. Since gate is negative, it means electrons are on the gate as shown is Fig. 19.47 (*ii*). These electrons repel the free electrons in the *n*-channel, leaving a layer of positive ions in a part of the channel as shown in Fig. 19.47 (*ii*). In other words, we have depleted (*i.e.* emptied) the *n*-channel of some of its free electrons. Therefore, lesser number of free electrons are made available for current conduction through the *n*-channel. This is the same thing as if the resistance of the channel is increased. The greater the negative voltage on the gate, the lesser is the current from source to drain. Thus by changing the negative voltage on the gate, we can vary the resistance of the *n*-channel and hence the current from source to drain. Note that with negative voltage to the gate, the action of *D-MOSFET* is similar to *JFET*. Because the action with negative gate depends upon depleting (*i.e.* emptying) the channel of free electrons, the negative-gate operation is called *depletion mode.*



(*ii*) Enhancement mode. Fig. (*i*) shows enhancement-mode operation of *n*-channel *DMOSFET*. Again, the gate acts like a capacitor. Since the gate is positive, it induces negative charges in the *n*-channel as shown in Fig. 19.48 (*ii*). These negative charges are the free electrons drawn into the channel. Because these free electrons are added to those already in the channel, the total number of free electrons in the channel is increased. Thus a positive gate voltage *enhances* or *increases* the conductivity of the channel. The greater the positive voltage on the gate, greater the conduction from source to drain. Thus by changing the positive voltage on the gate, we can change the conductivity of the channel. The main difference between *D-MOSFET* and *JFET* is that we can apply positive gate voltage to *D-MOSFET* and still have essentially zero current. Because the action with a positive gate depends upon *enhancing* the conductivity of the channel, the positive gate operation is called *enhancement mode.*



The following points may be noted about *D-MOSFET* operation :

(*i*) In a *D-MOSFET*, the source to drain current is controlled by the electric field of capacitor formed at the gate.

(*ii*) The gate of *JFET* behaves as a reverse-biased diode whereas the gate of a *D-MOSFET* acts like a capacitor. For this reason, it is possible to operate *D-MOSFET* with positive or negative gate voltage.

(*iii*) As the gate of *D-MOSFET* forms a capacitor, therefore, negligible gate current flows whether positive or negative voltage is applied to the gate. For this reason, the input impedance of *D-MOSFET* is very high, ranging from 10,000 MΩ to 10,000,00 MΩ.

(*iv*) The extremely small dimensions of the oxide layer under the gate terminal result in a very low capacitance and the *D-MOSFET* has, therefore, a very low input capacitance. This characteristic makes the *D-MOSFET* useful in high-frequency applications.

Static characteristics of enhancement MOSFET

The variation of drain current I_D with drain to source voltage V_{DS} with gate voltage V_{GS} maintained constant at a value greater than V_T, gives the drain characteristic of enhancement MOSFET. Fig. 9.7-3 shows a typical set of drain characteristics of an n-channel enhancement MOSFET.

When $V_{GS} < V_T$ no channel is formed between the source and drain, then the E-MOSFET is off and hence $I_D = 0$. Now consider the case when V_{GS} is maintained constant at a voltage greater than V_T and V_{DS} is increased gradually from 0V. When V_{DS} is small I_D increases almost linearly with V_{DS}. This is the linear ohmic region. In this region the enhancement MOSFET behaves like a resistor. The value of the resistance is controlled by the gate voltage V_{GS}. Theoretical analysis shows that the drain characteristics in the ohmic region can be represented by

$$I_D = k\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right] \qquad (9.7\text{-}1)$$

where k depends on the construction of the device. For small values of V_{DS} the above equation reduces to

$$I_D = 2k(V_{GS} - V_T)V_{DS} \qquad (9.7\text{-}2)$$

which gives drain current I_D to be proportional to V_{DS}.

As V_{GS} is increased the density of electrons in the channel increases. This in turn increases the channel conductivity and decreases the resistance between the source and drain. With a given V_{GS} as V_{DS} is increased the p-n transition region between the substrate and the drain becomes reverse-biased while the source to substrate voltage remains zero. The depletion layer at the drain transition region widens, the negative space charge established by acceptor ions increases and as a result the effective channel

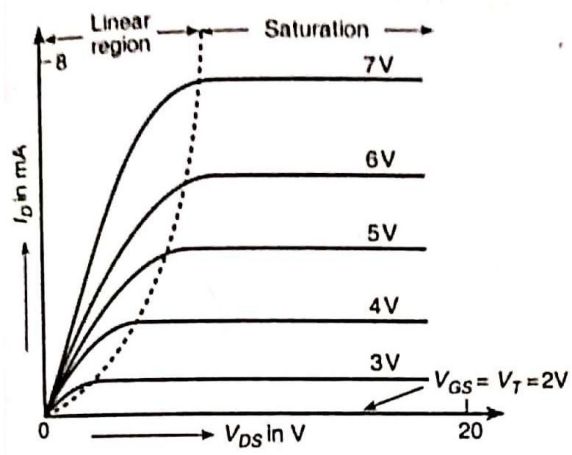


Fig. 9.7-3: Drain characteristics of typical enhancement NMOSFET

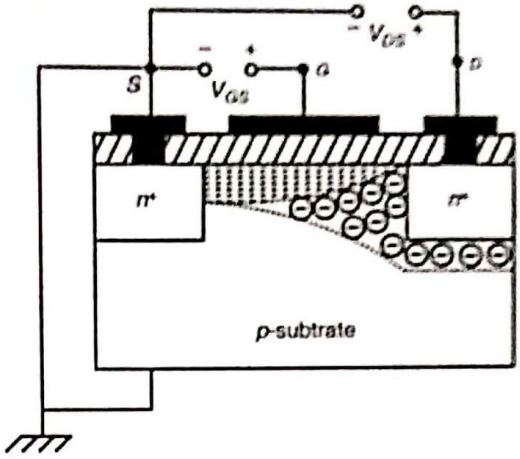


Fig. 9.7-4: Operation of enhancement MOSFET in the saturation region

cross-section decreases with increasing distance from the source (Fig. 9.7-4). This increases the channel resistance. When V_{DS} reaches a critical value the channel at the drain end becomes pinched off (actually a narrow strip). The current then becomes almost saturated. As V_{DS} rises further the beginning of the channel neck shifts towards the source and the channel resistance increases still more. This increment in channel resistance is not exactly in proportion to V_{DS}. As a result I_D somewhat increases with V_{DS}. For large enough V_{DS} there may be breakdown in enhancement MOSFET, causing sudden increase in I_D.

The dividing line between the ohmic and saturation regions (as shown by the dashed curve in Fig. 9.7-3) is given by

$$V_{DS} = V_{GS} - V_T \tag{9.7-3}$$

Substituting this in Eq. (9.7-1), we get

$$I_D = kV_{DS}^2 \tag{9.7-4}$$

Which gives drain current I_D is proportional to V_{DS}.

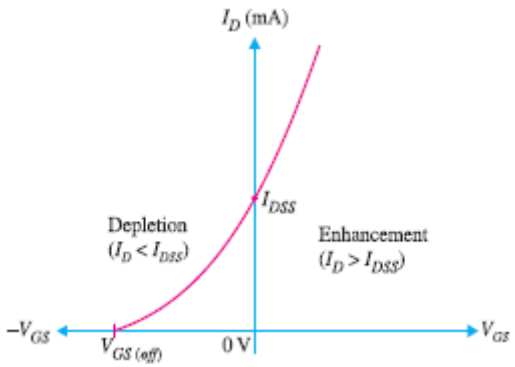
D-MOSFET Transfer Characteristic

Fig. 19.49 shows the transfer characteristic curve (or transconductance curve) for *n*-channel *D-MOSFET*.

The behaviour of this device can be beautifully explained with the help of this curve as under :

(*i*) The point on the curve where $V_{GS} = 0$, $I_D = I_{DSS}$. It is expected because I_{DSS} is the value of I_D when gate and source terminals are shorted *i.e.* *VGS* = 0.

(*ii*) As V_{GS} goes *negative*, *ID* decreases below the value of I_{DSS} till I_D reaches zero when V_{GS} = V_{GS} (*off*) just as with *JFET*.



(*iii*) When V_{GS} is *positive*, I_D increases above the value of I_{DSS}. The maximum allowable value of I_D is given on the data sheet of *D-MOSFET*

Note that the transconductance curve for the *D-MOSFET* is very similar to the curve for a *JFET*. Because of this similarity, the *JFET* and the *D-MOSFET* have the same transconductance equation viz.

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_{GS(off)}}\right)^2$$

Depletion MOSFET characteristic curves

Fig. shows typical drain characteristics of an n-channel MOSFET. To explain the curves we first consider the case with $V_{GS} = 0$. As a channel is already diffused between the source and the drain, the drain current I_D at first increases linearly with V_{DS}. This is the ohmic region where MOSFET behaves like a simple resistor.

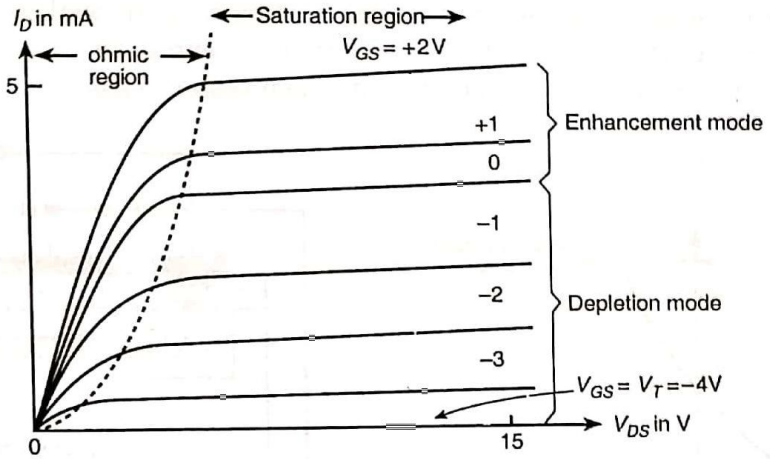


Fig. Drain characteristics of a typical n-channel depletion MOSFET

In this ohmic region I_D is shown to be given by

$$I_D = k\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right] \qquad (9.7\text{-}8)$$

where $k = I_{DSS}/V_T^2$. For small values of V_{DS} i.e., $V_{DS} \ll V_T$, the above equation reduces to

$$I_D = 2k(V_{GS} - V_T)V_{DS} \tag{9.7-9}$$

which shows that I_D is proportional to V_{DS}.

If V_{GS} is made negative it repels electrons from the channel to the bulk of the p-substrate and attracts holes to the channel. The result is a depletion of majority electrons in the channel. It thus reduces I_D for a given V_{DS}. The MOSFET is then said to operate in the *depletion mode.*

For a given V_{GS} if V_{DS} is increased I_D saturates. This is due to pinch off of the channel. The voltage drop along the channel due flow of I_D causes the channel more depleted near the drain than near the source (Fig. 9.7-10). As a result the current is forced to flow through a wedge-shaped channel. For certain value of V_{DS} the channel gets pinched off and I_D becomes saturated.

The dividing line between the ohmic and saturation regions is the locus of pinch-off and is given by

$$V_{DS} = V_{GS} - V_T \tag{9.7-10}$$

Substituting this in Eq. (9.7-8) we get

$$I_D = k V_{DS}^2 \tag{9.7-11}$$

It shows that the pinch-off locus is a parabola.

If a positive voltage is applied to the gate it attracts additional free electrons into the channel region. It enhances channel conductively and drain current above I_{DSS} The MOSFET is then said to be operating in *enhancement mode.*

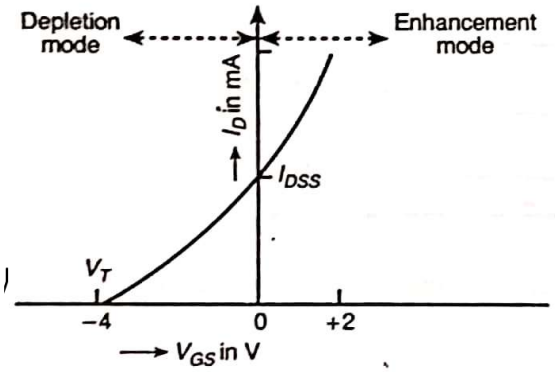


Fig. 9.7-9: Transfer characteristics of a typical n-channel depletion MOSFET

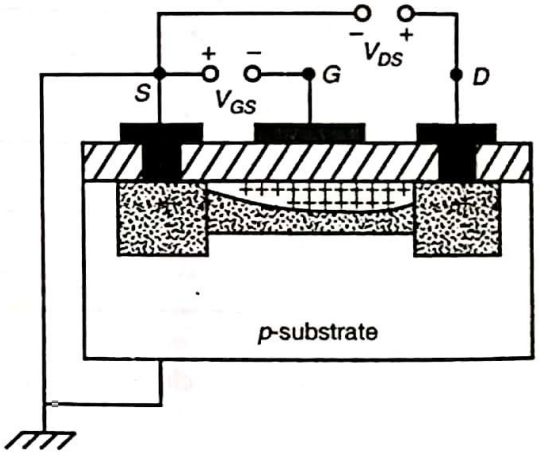


Fig. 9.7-10: MOSFET with a depleted channel

JFET as amplifier

Common source amplifier

A common source amplifier using an n-channel JFET is shown in Fig. This FET configuration is similar to common emitter configuration of bipolar junction transistor. Here, the a.c signal is connected in series with the battery V_{GG}, the gate bias. This causes a variation of v_{gs} to the total of gate-to-source voltage. Let the corresponding

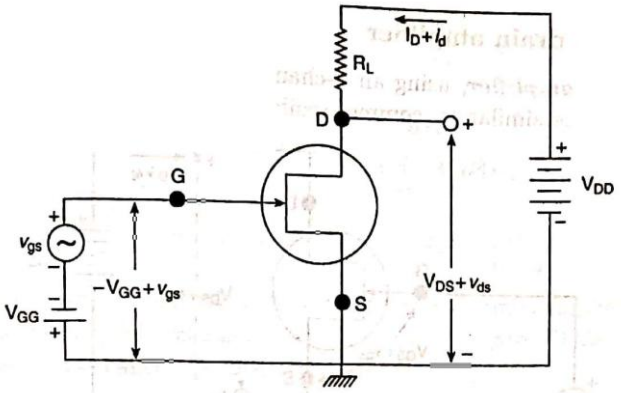


Fig. Common source amplifier

output voltage change be v_{ds} which appears across the load resistance R_L connected across the drain-source terminal. When no input signal is applied, we get from the output circuit

$$V_{DD} = V_{DS} + I_D R_L \tag{9.9.1}$$

But, using KVL for a.c and d.c components, we have

$$V_{DD} = V_{DS} + v_{ds} + (I_D + i_d)R_L \tag{9.9.2}$$

Subtracting equation (9.9.1) from (9.9.2), we obtain

$$i_d R_L + v_{ds} = 0 \tag{9.9.3}$$

For small signal voltages, equation (9.7.4) provides

$$i_d = g_m v_{gs} + \frac{v_{ds}}{r_d} \tag{9.9.4}$$

Substituting (9.9.4) in (9.9.3), we get

$$\left(g_m v_{gs} + \frac{v_{ds}}{r_d}\right) R_L + v_{ds} = 0$$

$$\text{or,} \quad \frac{v_{ds}}{v_{gs}} = -\frac{g_m R_L}{(1 + R_L/r_d)} = -\frac{g_m r_d R_L}{R_L + r_d}$$

$$= -\frac{\mu R_L}{R_L + r_d}, \quad (\because \mu = g_m r_d)$$

$\therefore$ Voltage gain, $$A_V = \frac{v_{ds}}{v_{gs}} = -\mu \frac{R_L}{R_L + r_d} \tag{9.9.5}$$

The negative sign indicates that input and output voltages *differ in phase* by π.

The output resistance is a parallel combination of a.c drain resistance r_d and the load resistance R_L.

$\therefore$ Output resistance, $$R_0 = \frac{R_L r_d}{R_L + r_d} \tag{9.9.6}$$

Common drain amplifier

A ***common drain amplifier***, using an n-channel JFET, is shown in Fig. 9.15. This FET configuration is similar to common collector configuration of bipolar junction

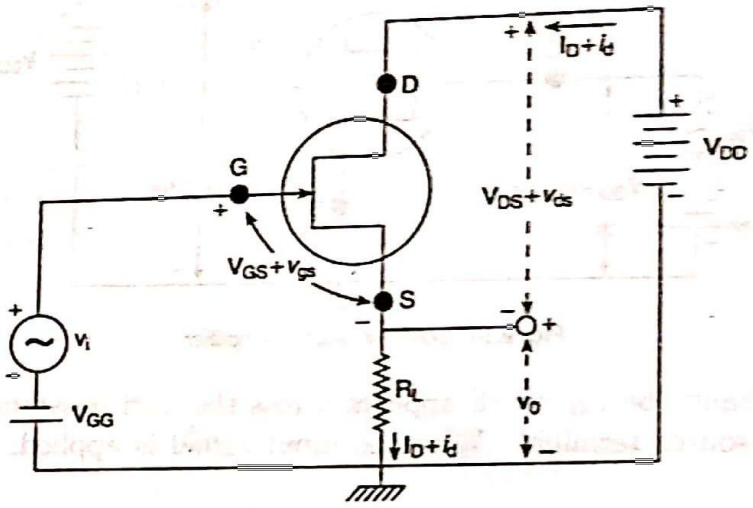


Fig. 9.15 Common drain amplifier

transistor. Here, v_i is the a.c input gate voltage and v_0 the corresponding output voltage appearing across the load R_L. The d.c and a.c components of voltages and currents are shown by usual notations.

Applying KVL to the output circuit for a.c component, we get

$$i_d R_L + v_{ds} = 0 \tag{9.9.7}$$

For small signal, we get $\quad i_d = g_m v_{gs} + \dfrac{v_{ds}}{r_d}$

$\therefore$ From (9.9.7), $\quad \left(g_m v_{gs} + \dfrac{v_{ds}}{r_d}\right) R_L + v_{ds} = 0 \tag{9.9.8}$.

Applying KVL to the input circuit a.c, we obtain

$$v_{gs} = v_i - i_d R_L = v_i + v_{ds}$$

$\therefore$ From (9.9.8), $\quad R_L \left[g_m(v_i + v_{ds}) + \dfrac{v_{ds}}{r_d}\right] + v_{ds} = 0$

$$\text{or,} \quad v_{ds}\left[1 + \frac{R_L}{r_d} + g_m R_L\right] = -g_m v_i R_L$$

$$\text{or,} \quad v_{ds} = -\frac{g_m r_d v_i R_L}{r_d + R_L + g_m r_d R_L}$$

$$= -\frac{\mu v_i R_L}{r_d + (1+\mu) R_L} \quad (\because \mu = g_m r_d)$$

Again, $v_0 = -v_{ds}$. $\therefore \quad -\frac{v_{ds}}{v_i} = \frac{v_0}{v_i} = \frac{\mu R_L}{r_d + (1+\mu)R_L}$

$\therefore$ Voltage gain is: $\boxed{A_V = \frac{\mu R_L}{r_d + (1+\mu)R_L}}$

$$\text{If } R_L \gg \frac{r_d}{1+\mu}, \text{ then } A_V = \frac{\mu}{1+\mu}.$$

In this case, if $\mu \gg 1$ then $A_V = 1$. The voltage gain unity implies that the output voltage (at the source) follows the input voltage (at the gate). This is why a common drain amplifier is also called a ***source follower.***

Complementary metal-oxide-semiconductor (CMOS)

Complementary metal-oxide-semiconductor, abbreviated CMOS, is a semiconductor technology used in manufacturing most of the microchips in modern computer. In CMOS, two types of enhancement MOSFETs (PMOS and NMOS) are interconnected in a complementary symmetry arrangement on the same substrate such that an increase in gate bias of the device enhances the conductivity between the drain and the source. Since the transistors are arranged in complementary symmetry, only one of the two MOSFETs is turned on at a time. So, power dissipation is controlled by the leakage currrent of the '*off*' transistor and it is of extremely low value. Hence, CMOS technique is preferred to conventional MOSFET circuits in critical power saving applications and fabrication of ICs.

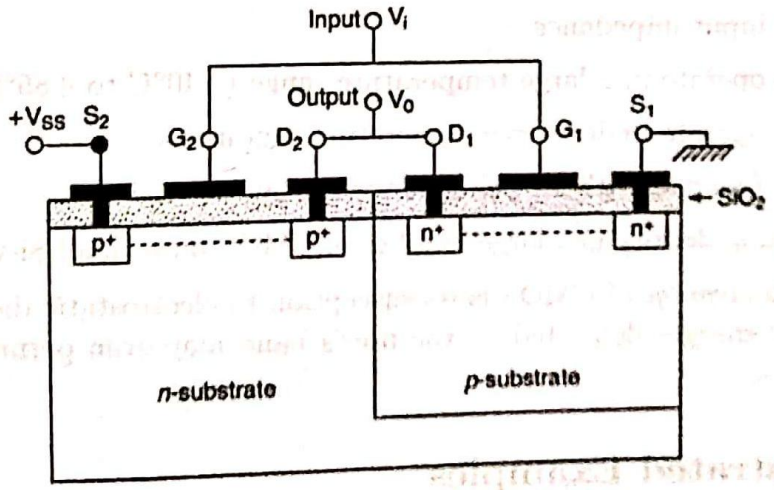


Fig. 9.16 Cross-sectional view of CMOS inverter

Fig. 9.16 shows a cross-sectional view of a simple CMOS inverter circuit consisting of a combination of NMOS and a PMOS on the same substrate. Fig. 9.17 shows the symbolic version of the same circuit.

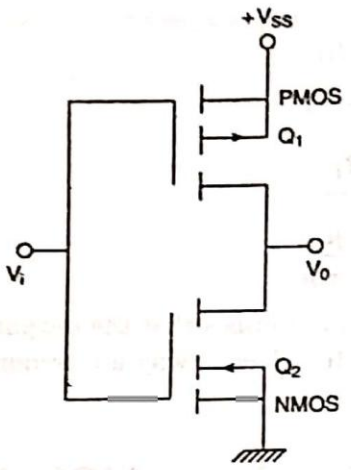


Fig. CMOS inverter circuit

Here, Q_1 is a PMOS where the source is connected to the applied voltage V_{SS} and Q_2 is an NMOS with source grounded. The gate terminals of both the MOSFETs are connected together to the input V_i while the drain terminals are connected together to form the output terminal V_0.

When the input V_i is high ($> V_T$), the transistor Q_2 (i.e., NMOS) is *on* and Q_1 (i.e., PMOS) is *off*. So, the output V_0 is low. On the other hand, when V_i is low, the transistor Q_1 is switched *on* but Q_2 becomes cut *off*. As a result, the output V_0 is high. Thus, in complementary symmetry configuration while one transistor is *on*, the other remains *off*.

Since the two transistors are in series, the drain current that flows is limited by the off transistor to the leakage value. So, the quiescent current practically does not flow and the power dissipation is caused only by the leakage current of the *off*-transistor. The power dissipation is thus virtually zero ($\sim$ a few nanowatt). The extremely low value of power dissipation or consumption of CMOS has led it to fabricate many other logic circuits—digital and analog.

Advantages and disadvantages

The CMOS has a number of *advantages* over other FETs. These are the following.

1. Extremely low power consumption,
2. Fast switching speed,
3. Very high input impedance.
4. Ability to operate in a large temperature range (−40°C to +85°C)
5. Ability to operate under varying operating conditions.
6. Ability to function without being disturbed by external noise.
7. High packing density i.e., large number of CMOS on a small Si-wafer.

The *only disadvantge* of CMOS is its susception to electrostatic discharging. Even the small static charges deposited on the user's hand may even permanently damage the device.

References

1. **Solid State Physics and Electronics A.B. Gupta & Nurul Islam**
2. **Fundamental Principles of Electronics B.Ghosh**
3. **Principles of Electronics V.K. Mehta & Rohit Mehta**