Total Pages : 4

End Semester Examination of Semester–I, 2015
Subject : BCA
Paper : 1112 (Digital Electronics)
Full Marks : 70
Time : 3 Hrs

The figures in the margin indicate the marks corresponding to the question

Candidates are requested to give their answers in their own word as far as practicable.

Illustrate the answers wherever necessary.

Group A

1. Answer **any five** questions : 5X2=10

   a) Show that $A\bar{B}+(\bar{A}+B)C=A\bar{B}+C$.

   b) Subtract 748 from 983 using 9's complement method.

   c) What is Ex-NOR gate?

   d) What is the number of flip-flops required for a MOD-10 ring counter.

   e) What is half-adder? Write its truth table.

   f) Write down the characteristic equation of S-R flip-flop.

   g) What do you mean by prime implicant?

   h) What is RAM and ROM.

Group B

Answer **any five** questions : 5X4=20

2. Explain briefly the characteristics of MOS logic and CMOS logic.
3. Design a 4-bit parallel-in parallel-out (PIPO) Shift Register.
4. Design a 2-bit Gray-Binary Converter using basic logic gates with proper truth table.
5. Realize the function $f(A, B, C) = \sum m(1, 3, 5, 6)$ by a multiplexer. Discuss the operation logic.
6. Draw a full adder circuit as combination of 2 half-address.
7. Give the truth table of a clocked SR flip flop constructed with NAND gates and explain the truth table.
8. Design a 4X2 priority encoder having highest priority to D3.

Group C

Answer **any four** questions : 4X10=40

9. a) Design a MOD-10 Synchronous binary UP counter using JK flip flop and necessary logic gates. 5

   b) Design a clocked R.S. flip-flop using NAND gates. Explain its principle of operation. 5

10. Write a short note **(any four)**: $2\frac{1}{2} \times 4 = 10$

    a) Tri-state in TTL family.

    b) Data lock-out in a counter.

    c) Ripple counter.

    d) Odd parity generator.

    e) DRAM.

    f) Universal Shift Register.

11. a) Using Karnaugh map method, minimize the following expression : 5

    $F(a, b, c, d) = \sum m(1, 5, 6, 12, 13, 14) + \sum d(2, 4)$

    b) Implement XOR gate using NAND gates & NOR gates, respectively. $2\frac{1}{2} + 2\frac{1}{2}$

12. a) What do you mean by synchronous asynchronous sequential circuits? Give examples. 2+2

    b) Explain the functionality of D-flip flop. Give the truth table & state diagram. 2+2+2

13. a) Design a combinational circuit where a control line input must have. The output = 8 bit input, when CONTROL is 0 and output = complement of 8 bit input when CONTROL is 1. 4

    b) Design the circuit with the primary gates for the following digital equation after solving with K-Map method $y = ABC + ACD + \bar{A}\bar{B}\bar{D} + AB\bar{C}D + \bar{A}\bar{B}\bar{C}\bar{D}$.

    4

c) $(-9)_{10} + (-3)_{10}$ implement it by 1's complement subtraction method. 2

14. a) Design an octal to binary encoder. 4

b) Use a MUX to implement the logic function $F = A \oplus B \oplus C$. 4

c) Design a 3x8 decoder with truth table. 3